# Appendix F

## SPHERES AVIONICS DESIGN

This appendix presents detailed descriptions of the SPHERES avionics. The SPHERES laboratory avionics sub-systems implements electronics for the satellites, communications with the control computer, metrology beacons, and a beacon tester. This appendix also presents the design of several expansion port items already in use. Each section presents the functional block diagram and the complete schematics (when applicable) for all the electronic components of the SPHERES laboratory:

- SPHERES nano-satellites
  - Power & control panel
  - Data processing unit (C6701 DSP / SMT375)
  - Metrology
  - Communications
  - Propulsion
  - Expansion Port
  - Internal beacon
- Laptop communications
- Metrology Beacons
- Metrology Beacon Tester
- Expansion Port Items

## F.1 SPHERES nano-satellites

The electronics of the SPHERES nano-satellites, shown in Figure F.1, are implemented in two primary "electronics stacks", with several peripheral electronic boards. The groupings are as follows (third level bullets indicate peripheral electronic boards which support the primary board of that stack):

- First stack (power & propulsion)
  - Power
    - Batteries (2x)
    - Power Switch
    - Circuit Breaker
    - Control Panel
  - Propulsion
    - Propulsion LEDs
- Second stack (data processing)
  - SMT375 (C6701 DSP)
  - Metrology (Motherboard 1)
    - Metrology 6 (ultrasound / IR)
    - Accelerometer Boards
    - On-board beacon
  - Communications (Mother board 2)
    - DR200x wireless boards (2x)
    - Expansion Port

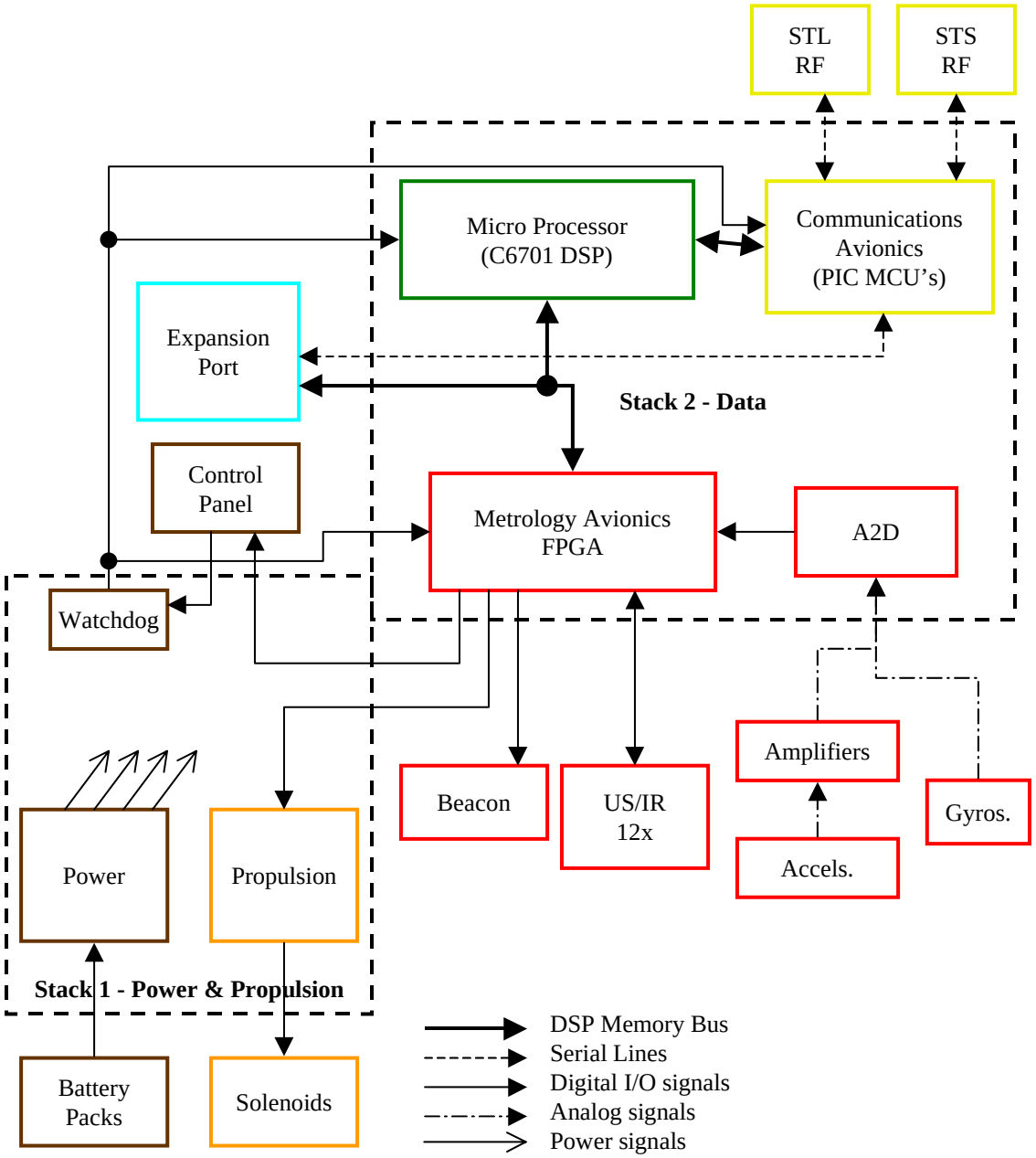



**Figure F.1** SPHERES avionics overview

## F.1.1 Power & Control Panel

### Design Drivers

- Provide the necessary power and voltages for all sub-systems
  - 3.3 V: DSP, Metrology, Communications
  - 5 V: DSP, Metrology, Communications, Propulsion
  - ±15 V: Metrology (gyros and accelerometers)
  - 22 V: Propulsion
- Meet applicable ISS safety guidelines
- Maximize battery utilization

### Functional Block Diagram

The power sub-system is comprised of three main type of electronic boards: battery packs, control panel, and the power regulation board. The circuit breaker and power switch are wired independently. The functional description, inputs, and outputs of each component are presented below.

### Battery packs

There are two types of battery packs: flight and rechargeable. The functions of the two types are:

- **Flight:** Provides up to two hours of operations to the SPHERES nano-satellites through 8 AA alkaline batteries. It also provides diode and fuse protection to meet NASA Safety requirements (triple redundancy).
- **Rechargeable:** Provides up to two hours of operations to the SPHERES nano-satellites through 8AA NiMH rechargeable batteries. The battery charging circuit resides within the packs themselves, requiring only a 15Vdc external supply. The external supply can have an optional LED to indicate charging status. The board provides the same diode and fuse protection as the flight packs.

Its inputs and outputs are listed in Table F.1

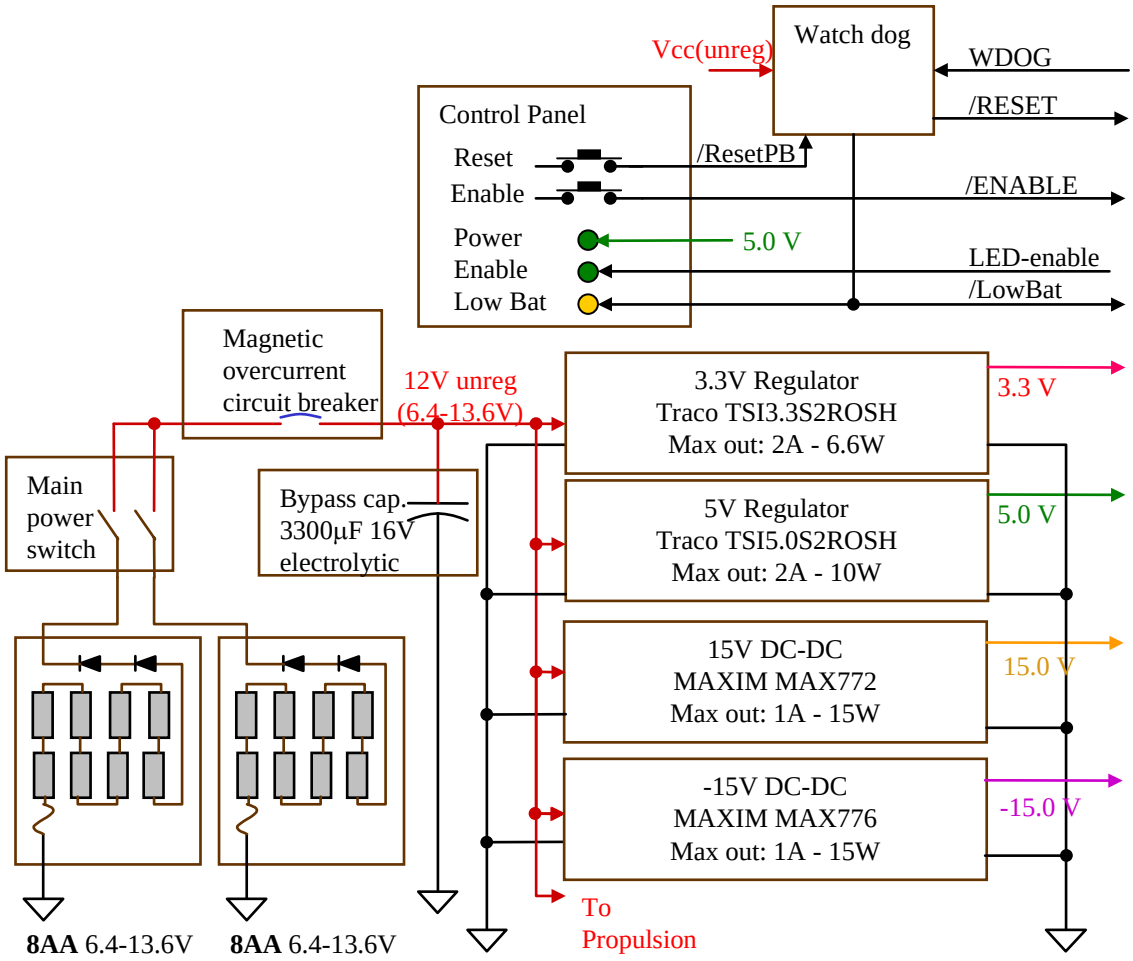



**Figure F.2** Power sub-system functional block diagram

### Power Switch

The power switch is a two phase mechanical switch. The switch is two phase so that the battery positive power connections are isolated when the switch is open (the SPHERES are off), preventing any current from flowing between the battery packs. While not necessary for NASA safety requirements, it allows the battery packs to remain inserted in the satellites without risk. Its inputs and outputs are listed in Table F.2

**TABLE F.1** Battery packs signals description

| Signal | Type | Description |
|---|---|---|
| Flight | | |
| Vin | In | Unregulated input voltage from 8AA batteries (6.4-13.6V) |
| Vout | Out | Protected, unregulated voltage (5.8-13.0V due to 0.6V drop through diodes) |
| GND | Pwr | Common reference ground |
| Rechargeable | | |
| Vin | In | Unregulated input voltage from 8AA batteries (6.4-13.6V) |
| Vout | Out | Protected, unregulated voltage (5.8-13.0V due to 0.6V drop through diodes) |
| Vsupply | In | 15V input voltage for recharging circuit |
| FT | Out | Signal to external LED which indicates charging in process (blinking) or done (solid on) |
| GND | Pwr | Common reference ground |

**TABLE F.2** Power Switch signals description

| Signal | Type | Description |
|---|---|---|
| | | Two phase power switch which isolates the battery packs when turned off |
| $Vin_1$, $Vin_2$ | In | Protected, unregulated voltage from battery packs |
| $Vout_1$, $Vout_2$ | Out | Switched, unregulated voltage to circuit breaker |

### Circuit Breaker

The magnetic circuit breaker provides 5A current protection. A thermistor is connected in series with the circuit breaker to prevent power-surges larger than 5A when the satellites are turned on and the large bypass capacitor (3300μF) charges. Once heated the thermistor has a resistance of approximately 0.1Ω. The inputs and outputs of this board are listed in Table F.3

**TABLE F.3** Circuit breaker signals description

| Signal | Type | Description |
|---|---|---|
| $Vin_1$, $Vin_2$ | In | Switched, unregulated voltage from power switch |
| Vout | Out | Switched and protected, unregulated voltage to power board |

### Control Panel

The control panel is the primary manual interface of the satellites. The panel mechanically holds the power switch, although it is not connected electrically. The panel electronics only include digital I/O lines powered through the regulated 5V supply. The elements in the panel are:

- Reset button - creates a negative logic signal which connects directly to the watchdog module, which in turn generates a correctly timed reset signal for the rest of the electronics.
- Enable button - creates a negative logic signal which is sent directly to the SPHERES FPGA as a general I/O signal; the SPHERES Core Software checks the state of this button to enable operations (go from "idle" to "ready" or "running" mode).
- Power LED - driven directly off the regulated 5V supply indicates when the power is on; since it is driven directly off the 5V supply, it is only on when the supply operates correctly, giving a reasonable indication that the power regulation module is operating correctly.
- Low Battery LED - the watchdog measures the unregulated battery voltage and indicates a low battery condition when there are approximately 20 minutes remaining of operation.
- Enabled LED - the LED is driven directly off the SPHERES FPGA as a general I/O signal; it is turned on by the SPHERES Core Software when the satellites are in a "ready" or "running".

The inputs and outputs of this board are listed in Table F.4

### Power Regulation Board

The power regulation board is the most complex board of the power sub-system. It provides power regulation for the data stack and all other avionics[1], contains the watchdog, and serves as a bypass for the propulsion signals. The board outputs four voltages to the

**TABLE F.4** Control panel signals description

| Signal | Type | Description |
|---|---|---|
| Vcc | Pwr | Input +5V dc |
| GND | Pwr | Common reference ground |
| LED-enable | In | Enable LED control signal |
| LED-lowbat | In | Low battery LED indicator control signal |
| /Reset | Out | Reset signal to power board watchdog module |
| /Enable | Out | Enable signal for SPHERES FPGA |

second stack: +3.3V, +5V, +15V, and -15V. The +3.3V and +5V signals are used throughout the system to power electronic components. The ±15V powers the accelerometers and gyroscopes. The power board is the mechanical attachment point for two of the gyroscopes, although no electrical signals from the gyroscopes pass through the board. Table F.5 lists the inputs and outputs of this board (or refers to other tables as applicable).

**TABLE F.5** Power regulation board signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Power to second electronic stack* | Vcc(+5V) | Pwr | +5V output |
| | Vcc(+3.3V) | Pwr | +3.3V output |
| | Vcc(+15V) | Pwr | +15V output |
| | Vcc(-15V) | Pwr | -15V output |
| | GND | Pwr | Common ground |
| *Data connector to second electronics stack* | THR 1-12 | In | Pass through signals for thrusters 1-12 |
| | /Enable | Out | Enable button pass through signal |
| | /LED-enable | In | Enable LED pass through signal |
| | /Batlow | Out | Low battery output to DSP |
| | WDOG | In | Watchdog control signal from DSP |
| | /RESET | Out | Reset control line to second electronics stack |

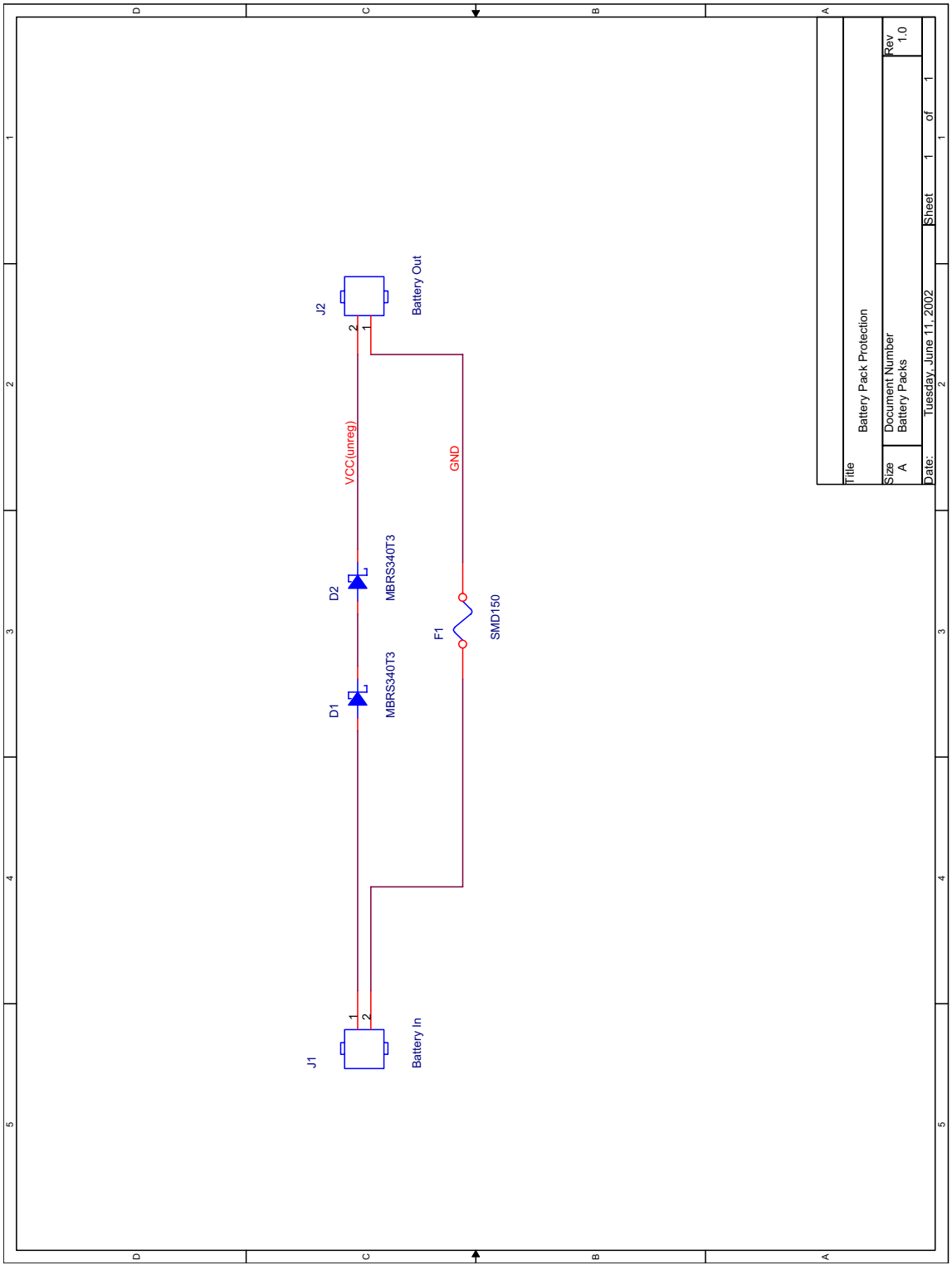
1. The propulsion sub-system increases the unregulated voltage to 20V; the power board does not provide the higher voltage required by the propulsion circuit.

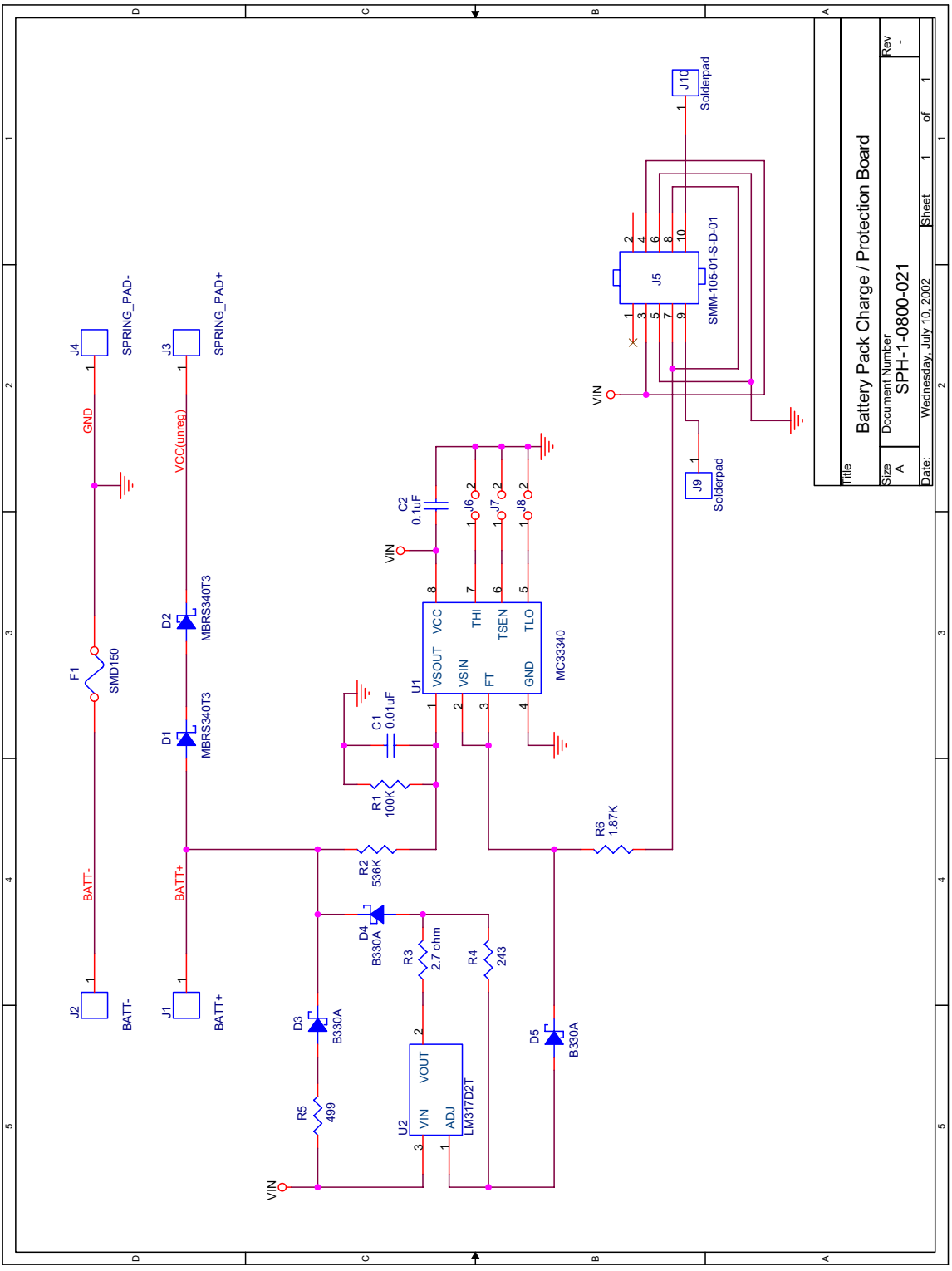
**TABLE F.5** Power regulation board signals description

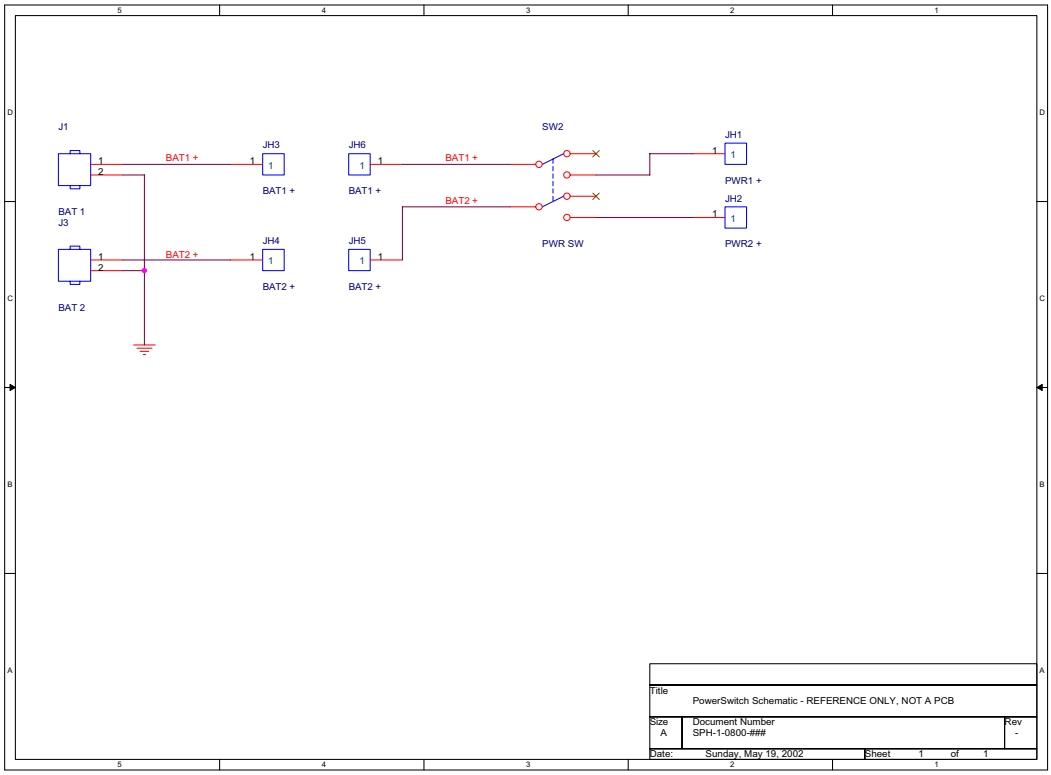
| Section | Signal | Type | Description |
|---|---|---|---|
| *Data and power to propulsion board* | THR 1-12 | Out | Pass through signals for thrusters 1-12 |
| | Vcc(5V) | Pwr | 5V power for propulsion board |
| | Vcc(unreg) | Pwr | Switched, protected, unregulated voltage for propulsion board |
| | GND | Pwr | Common ground |
| *Data to/ from control panel* | See Table F.4 | | |

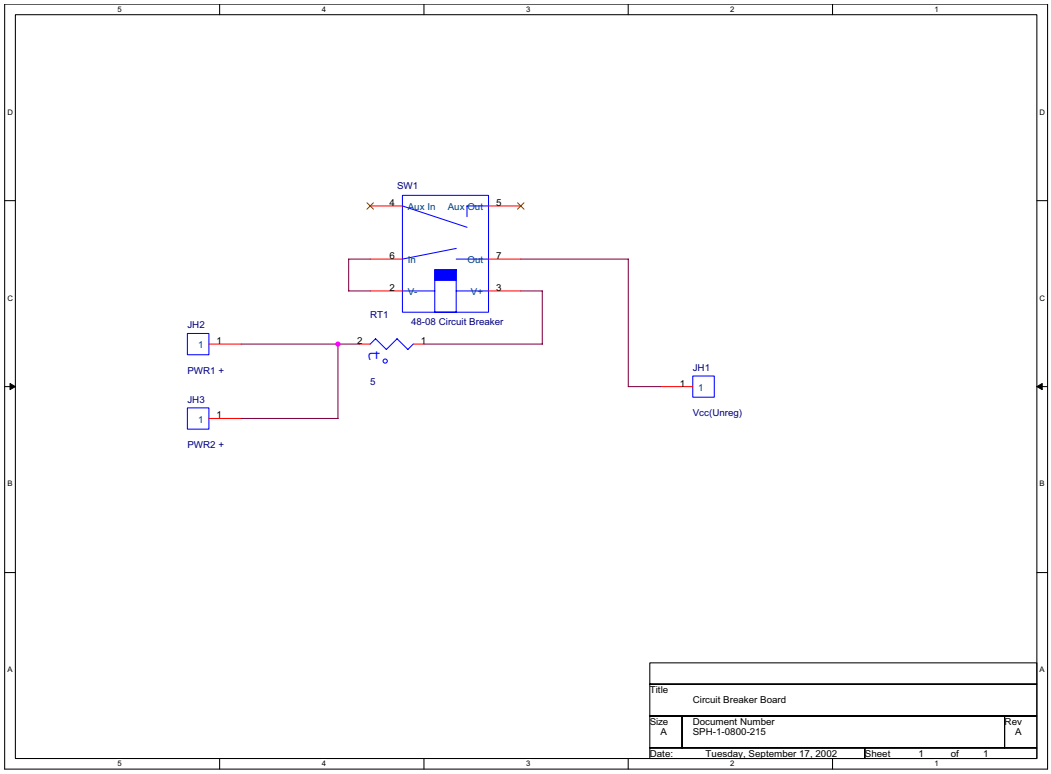
## Schematics

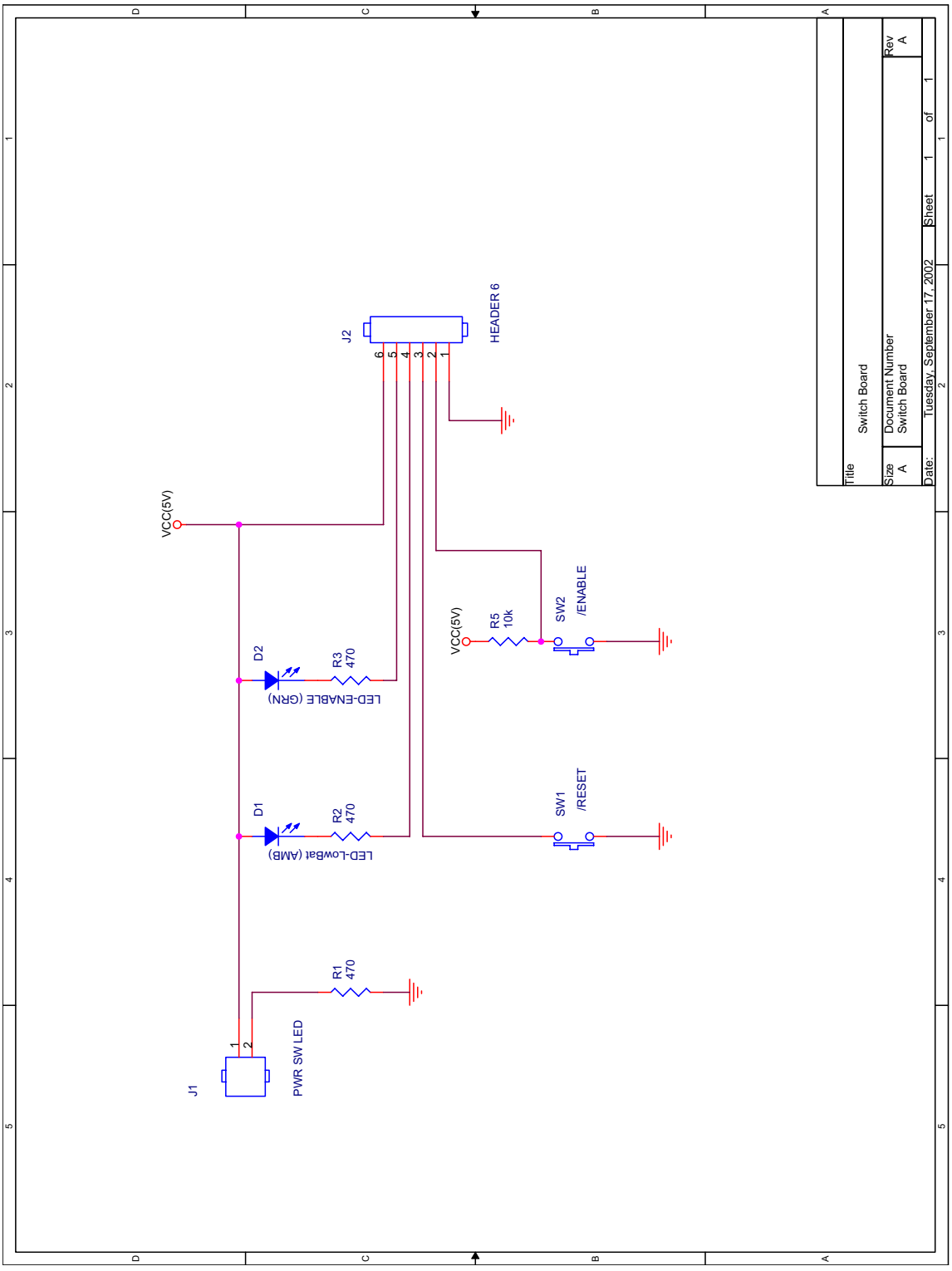
The schematics of the power sub-systems follow.

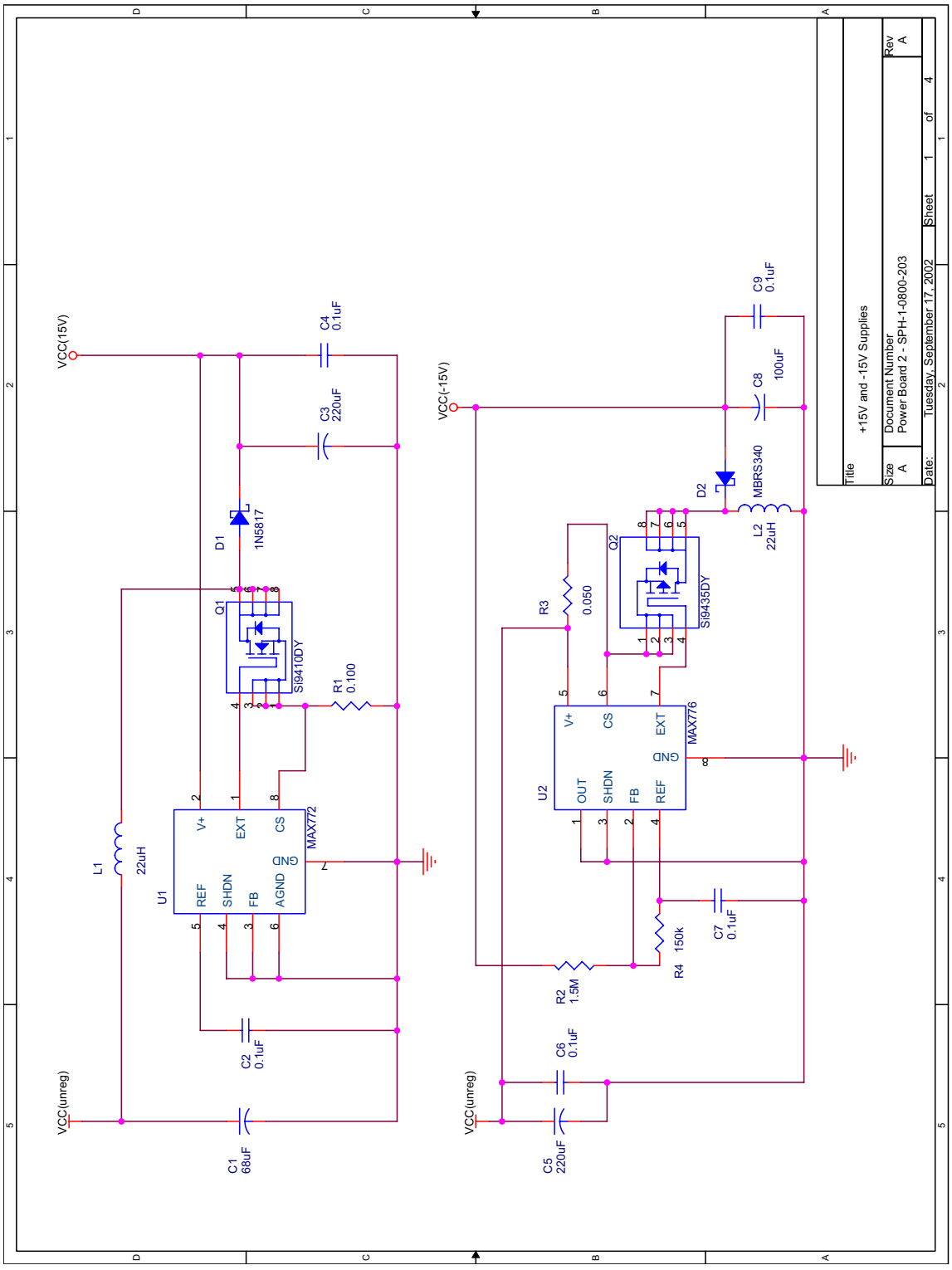

J2
Battery Out
2
1
VCC(unreg)
GND
D2
MBRS340T3
F1
SMD150
D1
MBRS340T3
1
2
J1
Battery In
Title
Battery Pack Protection
Size
A
Document Number
Battery Packs
Rev
1.0
Date:
Tuesday, June 11, 2002
Sheet
1
of
1

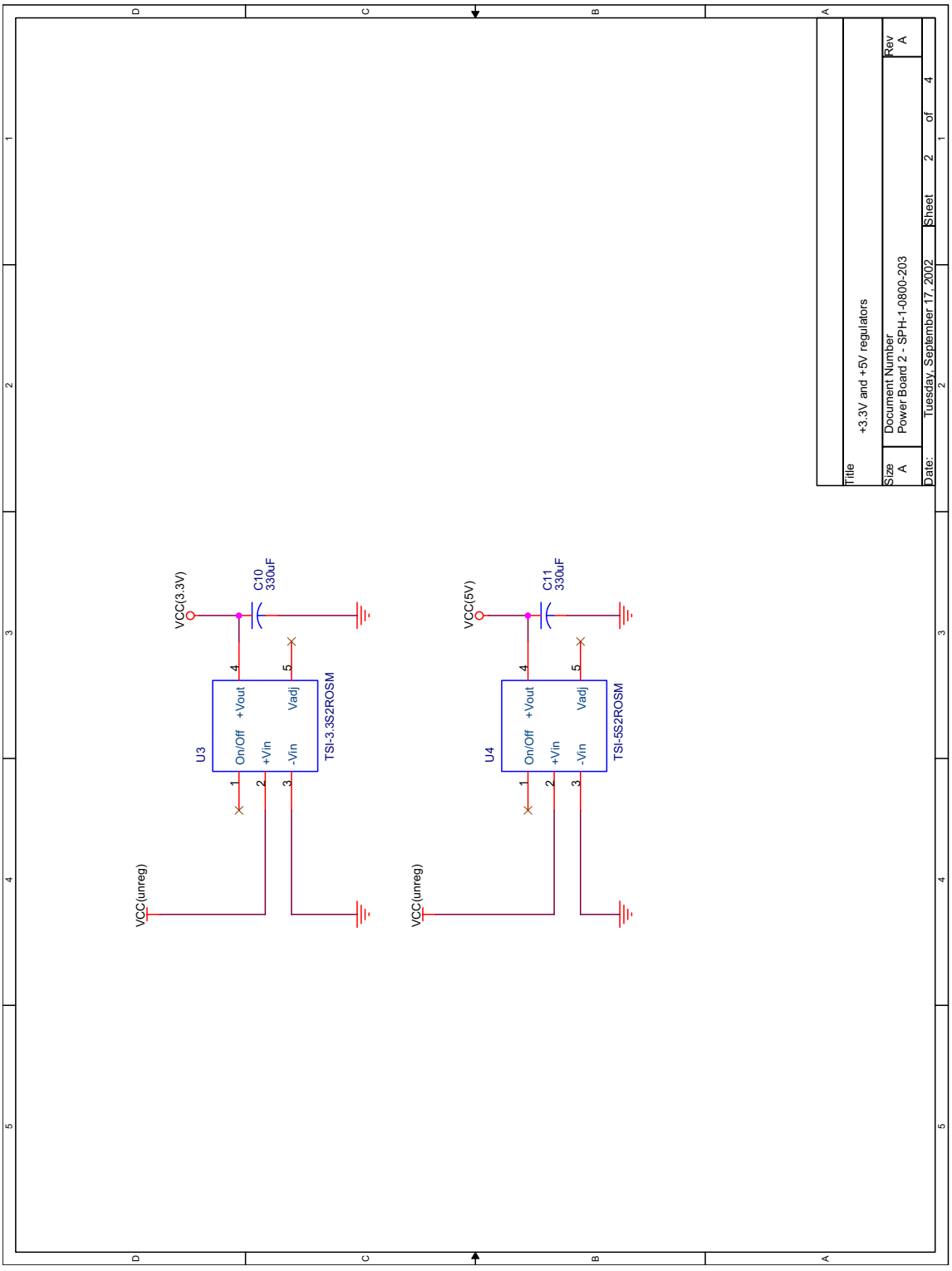

Title
Battery Pack Charge / Protection Board
Size
A
Document Number
SPH-1-0800-021
Rev
-
Date:
Wednesday, July 10, 2002
Sheet
1
of
1
J1
BATT+
J2
BATT-
J3
SPRING_PAD+
J4
SPRING_PAD-
J5
SMM-105-01-S-D-01
J6
J7
J8
J9
Solderpad
J10
Solderpad
F1
SMD150
D1
MBRS340T3
D2
MBRS340T3
D3
B330A
D4
B330A
D5
B330A
U1
MC33340
VSOUT
VSIN
FT
GND
VCC
THI
TSEN
TLO
U2
LM317D2T
VIN
VOUT
ADJ
R1
100K
R2
536K
R3
2.7 ohm
R4
243
R5
499
R6
1.87K
C1
0.01uF
C2
0.1uF
VIN
VCC(unreg)
GND
BATT+
BATT-

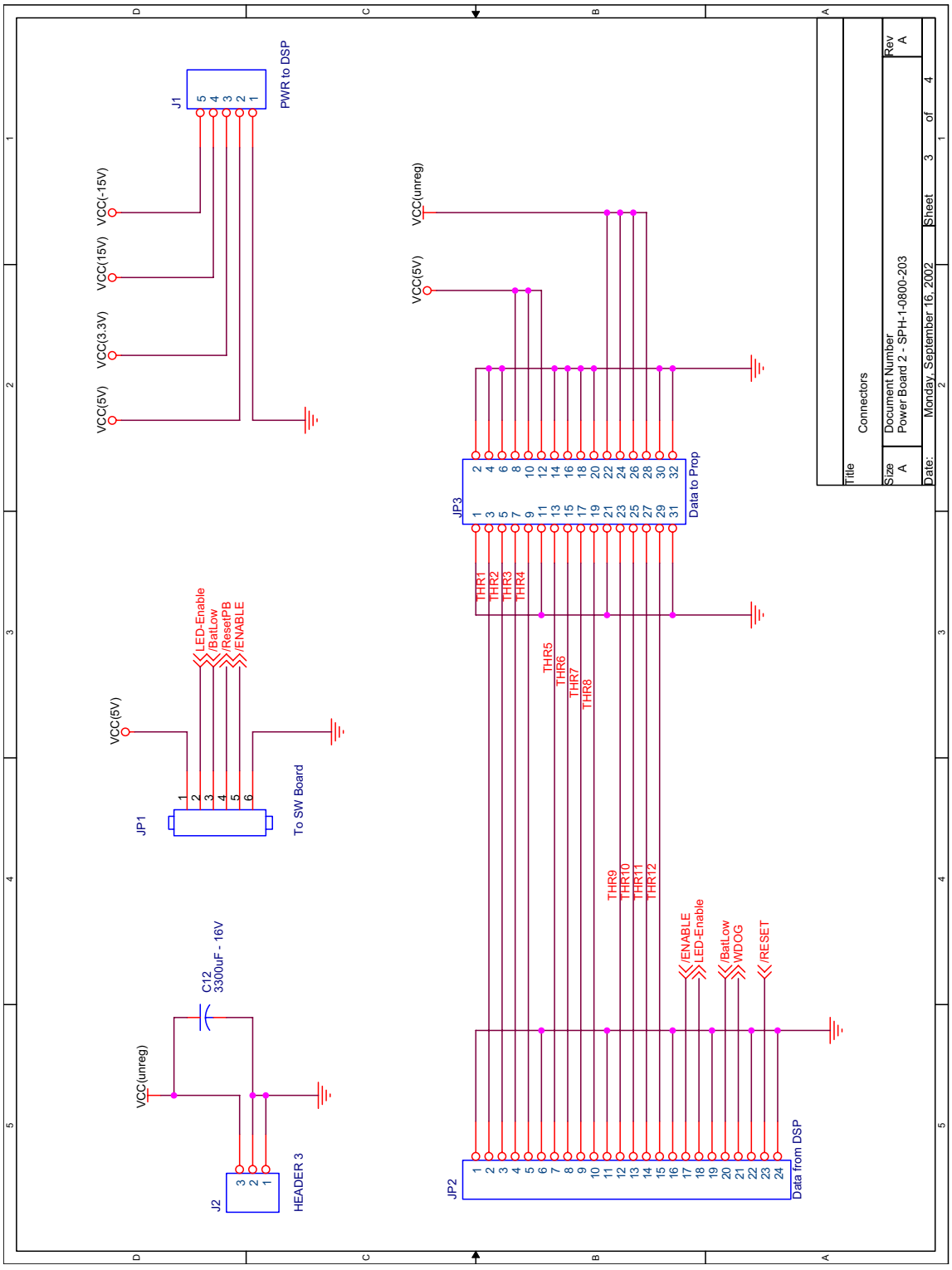

J1
BAT 1
J3
BAT 2
BAT1 +
BAT2 +
JH3
JH4
JH6
JH5
SW2
PWR SW
JH1
JH2
PWR1 +
PWR2 +
Title
PowerSwitch Schematic - REFERENCE ONLY, NOT A PCB
Size
A
Document Number
SPH-1-0800-###
Rev
-
Date: Sunday, May 19, 2002
Sheet 1 of 1

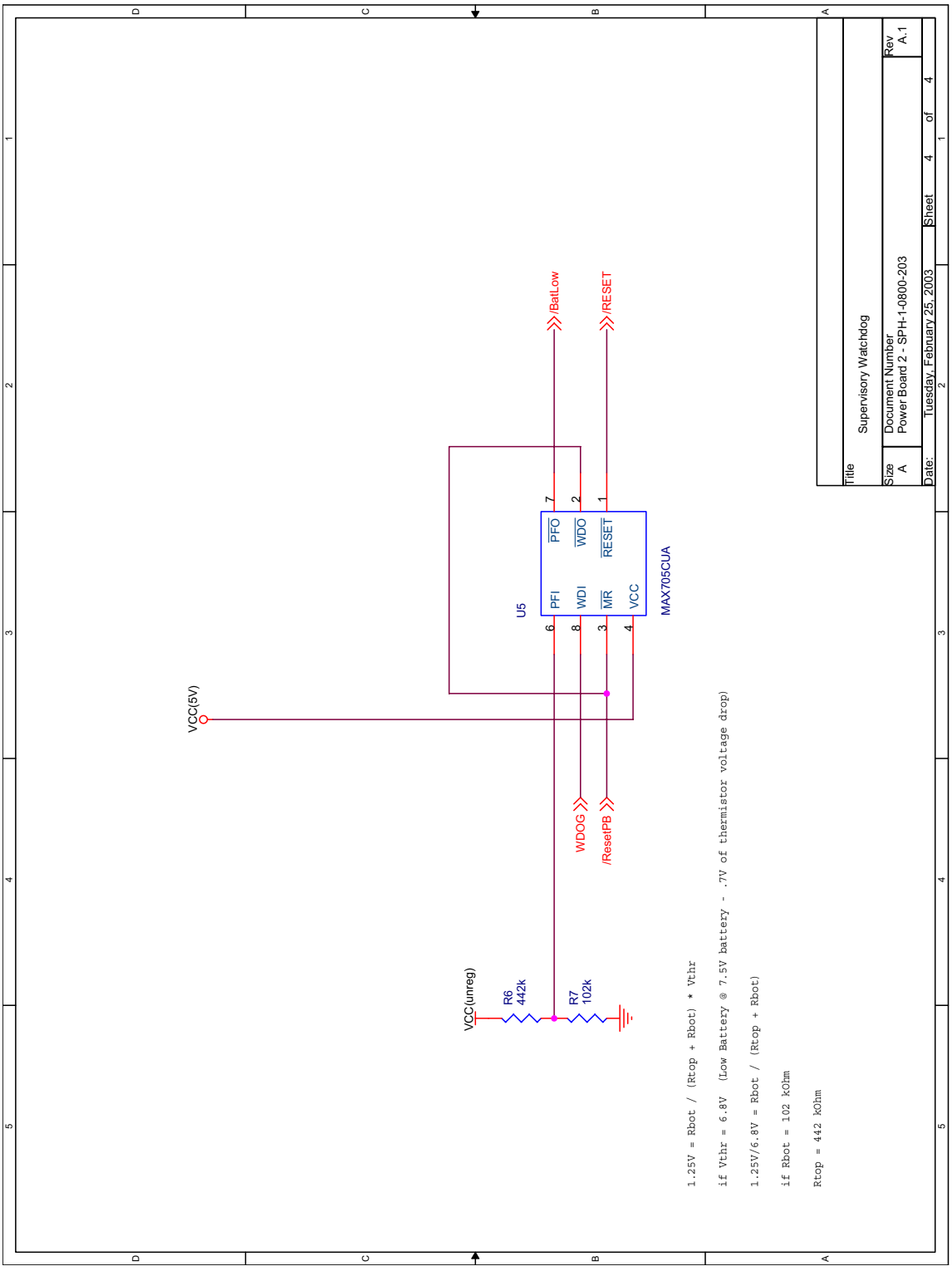

SW1
Aux In
Aux Out
In
Out
V-
V+
RT1
48-08 Circuit Breaker
JH2
PWR1 +
JH3
PWR2 +
JH1
Vcc(Unreg)
Title
Circuit Breaker Board
Size
A
Document Number
SPH-1-0800-215
Rev
A
Date: Tuesday, September 17, 2002
Sheet 1 of 1


Title
Switch Board
Size
A
Document Number
Switch Board
Rev
A
Date:
Tuesday, September 17, 2002
Sheet
1
of
1
J2
HEADER 6
6
5
4
3
2
1
VCC(5V)
D2
R3
470
LED-ENABLE (GRN)
VCC(5V)
R5
10k
SW2
/ENABLE
D1
R2
470
LED-LowBat (AMB)
SW1
/RESET
R1
470
J1
PWR SW LED
1
2


VCC(15V)
C4 0.1uF
C3 220uF
D1 1N5817
Q1 Si9410DY
R1 0.100
U1 MAX772
V+ EXT CS GND REF SHDN FB AGND
L1 22uH
C2 0.1uF
C1 68uF
VCC(unreg)
VCC(-15V)
C9 0.1uF
C8 100uF
D2 MBRS340
L2 22uH
Q2 Si9435DY
R3 0.050
U2 MAX776
V+ CS EXT GND OUT SHDN FB REF
R2 1.5M
R4 150k
C7 0.1uF
C6 0.1uF
C5 220uF
Title +15V and -15V Supplies
Size A
Document Number Power Board 2 - SPH-1-0800-203
Rev A
Date: Tuesday, September 17, 2002
Sheet 1 of 4


Title
+3.3V and +5V regulators
Size
A
Document Number
Power Board 2 - SPH-1-0800-203
Rev
A
Date:
Tuesday, September 17, 2002
Sheet
2
of
4
VCC(3.3V)
C10
330uF
U3
On/Off
+Vout
Vadj
+Vin
-Vin
TSI-3.3S2ROSM
VCC(unreg)
VCC(5V)
C11
330uF
U4
On/Off
+Vout
Vadj
+Vin
-Vin
TSI-5S2ROSM
VCC(unreg)


J1
PWR to DSP
VCC(-15V)
VCC(15V)
VCC(3.3V)
VCC(5V)
VCC(unreg)
VCC(5V)
JP3
Data to Prop
THR1
THR2
THR3
THR4
THR5
THR6
THR7
THR8
THR9
THR10
THR11
THR12
/ENABLE
LED-Enable
/BatLow
WDOG
/RESET
JP2
Data from DSP
LED-Enable
/BatLow
/ResetPB
/ENABLE
JP1
To SW Board
C12
3300uF - 16V
J2
HEADER 3
Title
Connectors
Size
A
Document Number
Power Board 2 - SPH-1-0800-203
Rev
A
Date:
Monday, September 16, 2002
Sheet
3
of
4


Supervisory Watchdog
Document Number
Power Board 2 - SPH-1-0800-203
Rev
A.1
Size
A
Date: Tuesday, February 25, 2003
Sheet 4 of 4
Title
U5
MAX705CUA
PFI
WDI
MR
VCC
PFO
WDO
RESET
/BatLow
/RESET
WDOG
/ResetPB
VCC(5V)
VCC(unreg)
R6
442k
R7
102k
1.25V = Rbot / (Rtop + Rbot) * Vthr
if Vthr = 6.8V (Low Battery @ 7.5V battery - .7V of thermistor voltage drop)
1.25V/6.8V = Rbot / (Rtop + Rbot)
if Rbot = 102 kOhm
Rtop = 442 kOhm

## F.1.2 Propulsion

### Design Drivers

- Create a *spike and hold* signal for the solenoids as presented in Figure F.3
  - Spike at +22V
  - Spike hold time: 7ms
  - Hold at +5V
  - Minimum impulse bit: 5ms
  - Maximum impulse bit: infinite
- Provide visual indication of solenoid states (open or closed)

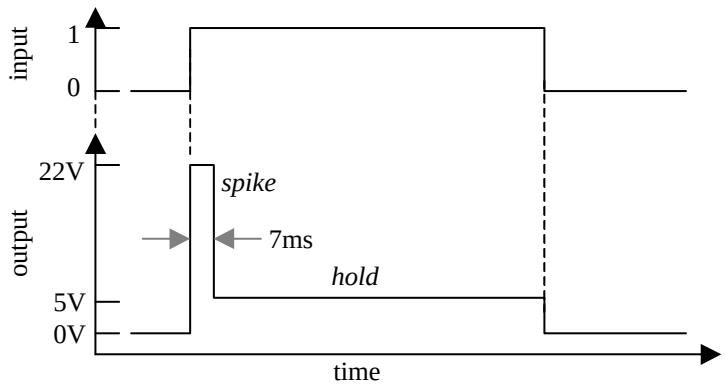



**Figure F.3** Propulsion *spike and hold* timing diagram

### Functional Block Diagram

Figure F.4 presents the functional block diagram of the propulsion system. A propulsion board receives the propulsion inputs from the data processing stack (pass through in the power board) and creates a spike and hold signal independently for each solenoid. The driver signals are sent to the solenoid via shielded wire to reduce the EMI effects of the spike on other circuits. A board with an LED attaches to the front face of the nozzle of each solenoid to indicate its state (off = closed, on = open). The propulsion board creates the +22V supply needed for the spike from the unregulated voltage input.

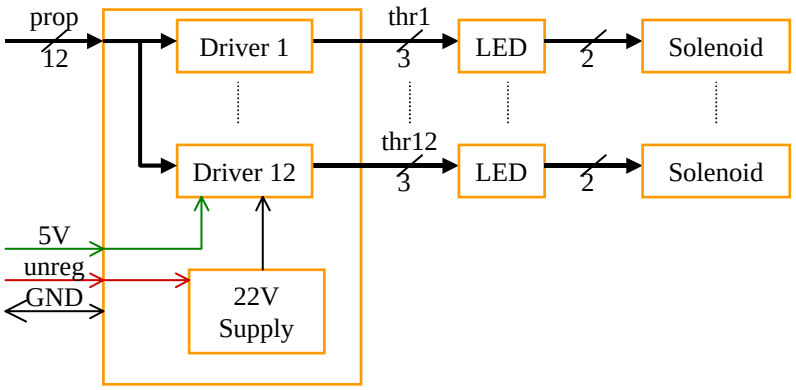



**Figure F.4** Propulsion avionics functional block diagram

### Propulsion Board

The propulsion board creates the spike and hold signal necessary to operate the solenoids. The board utilizes a Maxim MAX668 step-up switching regulator to create 22V from the variable 8-13V unregulated input. Each spike and hold circuit uses the schematic presented in Figure F.5 (with the necessary current limiting resistors and reverse voltage protection diodes). The inputs and outputs of this board are described in Table F.6.

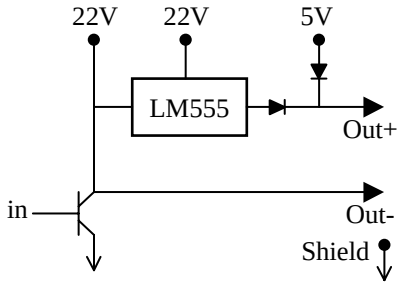



**Figure F.5** Propulsion *spike and hold* circuit

### Solenoid Board

The solenoid boards provide visual indication of the state of their corresponding solenoid. Their small size allows them to be mounted directly on top of the connector side of each nozzle, ensuring immediate correlation between an LED and a solenoid. The inputs and outputs of this board are listed in Table F.7.

**TABLE F.6** Propulsion board signals description

| Signal | Type | Description |
|---|---|---|
| GND | Pwr | Common ground |
| Vcc(5V) | Pwr | +5V supply |
| Vcc(unreg) | Pwr | Unregulated (8-13V) power |
| Prop[1-12] | In | Command signals from the data processing stack |
| PosDriver[1-12] | Out | Positive terminal for each solenoid |
| NegDriver[1-12] | Out | Negative terminal for each solenoid |

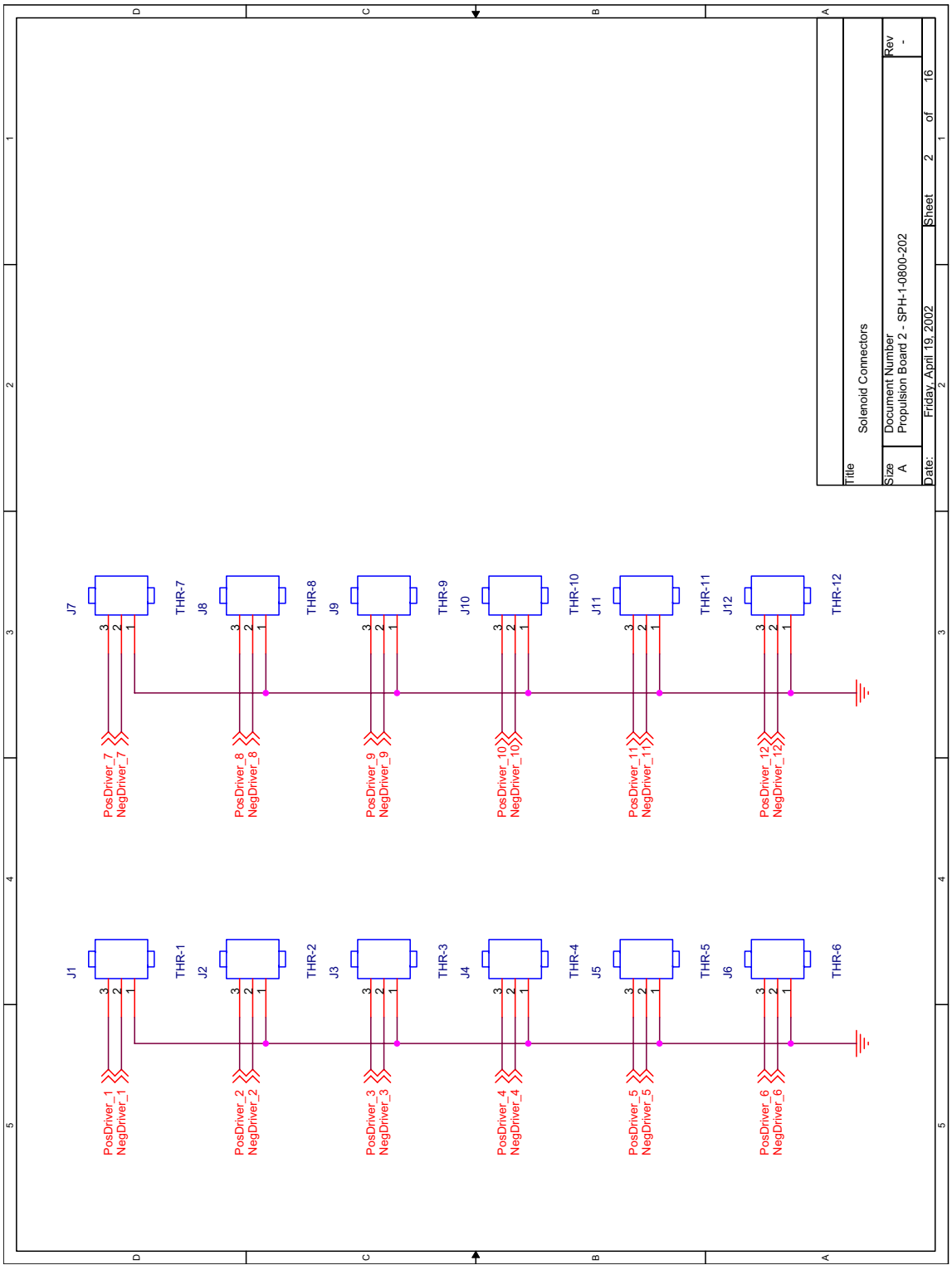
**TABLE F.7** Solenoid board signals description

| Signal | Type | Description |
|---|---|---|
| Thr + | I/O | Positive terminal of signal / solenoid |
| Thr - | I/O | Negative terminal of signal / solenoid |

### Schematics

The schematics for the propulsion sub-system follow.


PosDriver_1
NegDriver_1
PosDriver_2
NegDriver_2
PosDriver_3
NegDriver_3
PosDriver_4
NegDriver_4
PosDriver_5
NegDriver_5
PosDriver_6
NegDriver_6
PosDriver_7
NegDriver_7
PosDriver_8
NegDriver_8
PosDriver_9
NegDriver_9
PosDriver_10
NegDriver_10
PosDriver_11
NegDriver_11
PosDriver_12
NegDriver_12
Driver_1
Driver_2
Driver_3
Driver_4
Driver_5
Driver_6
Driver_7
Driver_8
Driver_9
Driver_10
Driver_11
Driver_12
PropIn
PropOut+
PropOut-
Drivers
thr1
thr2
thr3
thr4
thr5
thr6
thr7
thr8
thr9
thr10
thr11
thr12
Title
Firing Circuit Layout
Size
A
Document Number
Propulsion Board 2 - SPH-1-0800-202
Rev
-
Date:
Friday, April 19, 2002
Sheet
1
of
16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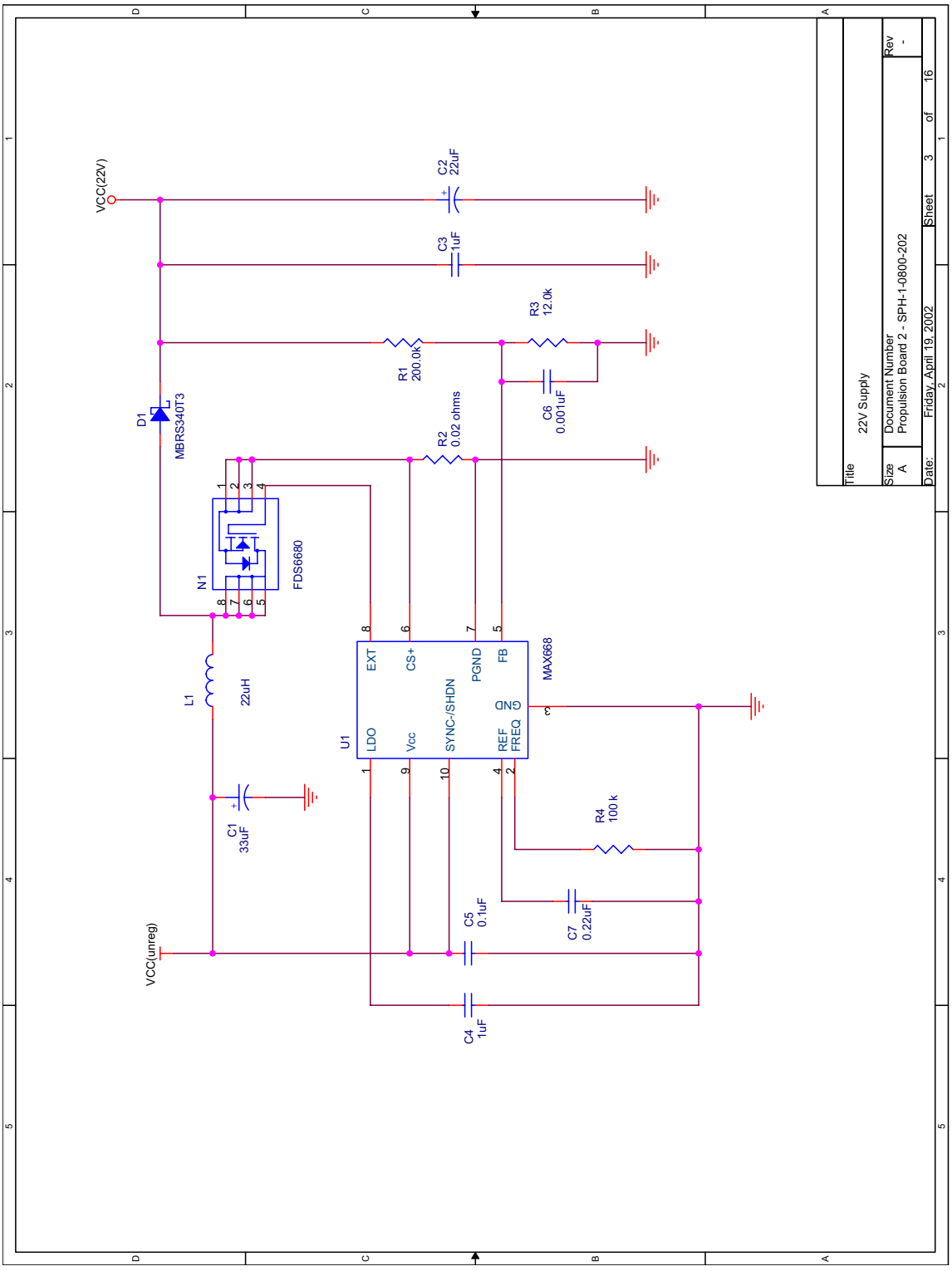
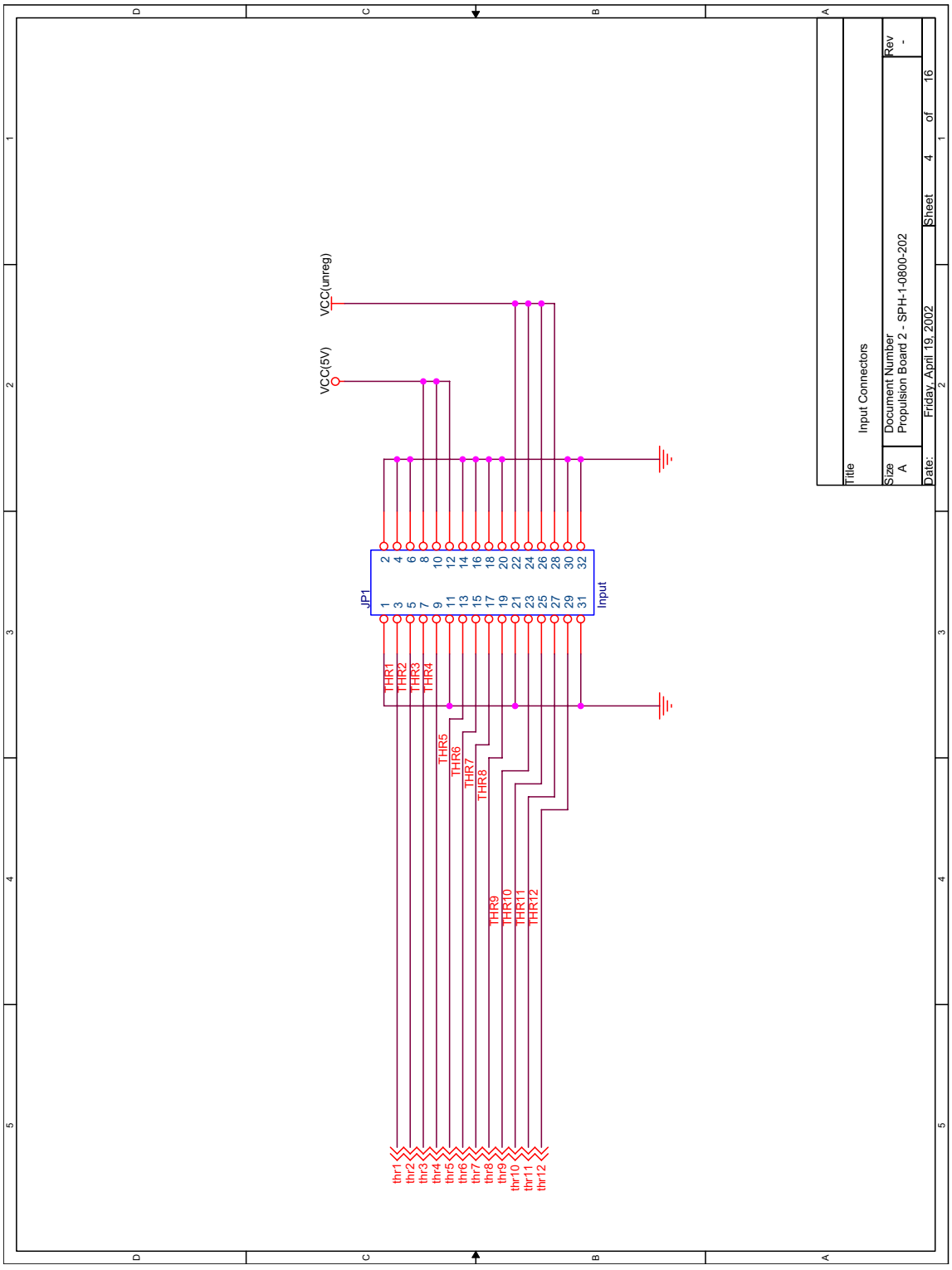
Solenoid Connectors
Size
A
Document Number
Propulsion Board 2 - SPH-1-0800-202
Rev
-
Date:
Friday, April 19, 2002
Sheet
2
of
16
J1
THR-1
J2
THR-2
J3
THR-3
J4
THR-4
J5
THR-5
J6
THR-6
J7
THR-7
J8
THR-8
J9
THR-9
J10
THR-10
J11
THR-11
J12
THR-12
PosDriver_1
NegDriver_1
PosDriver_2
NegDriver_2
PosDriver_3
NegDriver_3
PosDriver_4
NegDriver_4
PosDriver_5
NegDriver_5
PosDriver_6
NegDriver_6
PosDriver_7
NegDriver_7
PosDriver_8
NegDriver_8
PosDriver_9
NegDriver_9
PosDriver_10
NegDriver_10
PosDriver_11
NegDriver_11
PosDriver_12
NegDriver_12


VCC(22V)
C2 22uF
C3 1uF
R3 12.0k
R1 200.0k
C6 0.001uF
D1
MBRS340T3
R2 0.02 ohms
N1
FDS6680
L1
22uH
U1
MAX668
EXT
CS+
PGND
FB
LDO
Vcc
SYNC-/SHDN
GND
REF
FREQ
R4 100 k
C1 33uF
C5 0.1uF
C7 0.22uF
C4 1uF
VCC(unreg)
Title
22V Supply
Size A
Document Number
Propulsion Board 2 - SPH-1-0800-202
Rev -
Date: Friday, April 19, 2002
Sheet 3 of 16


VCC(unreg)
VCC(5V)
JP1
Input
THR1
THR2
THR3
THR4
THR5
THR6
THR7
THR8
THR9
THR10
THR11
THR12
thr1
thr2
thr3
thr4
thr5
thr6
thr7
thr8
thr9
thr10
thr11
thr12
Title
Input Connectors
Size
A
Document Number
Propulsion Board 2 - SPH-1-0800-202
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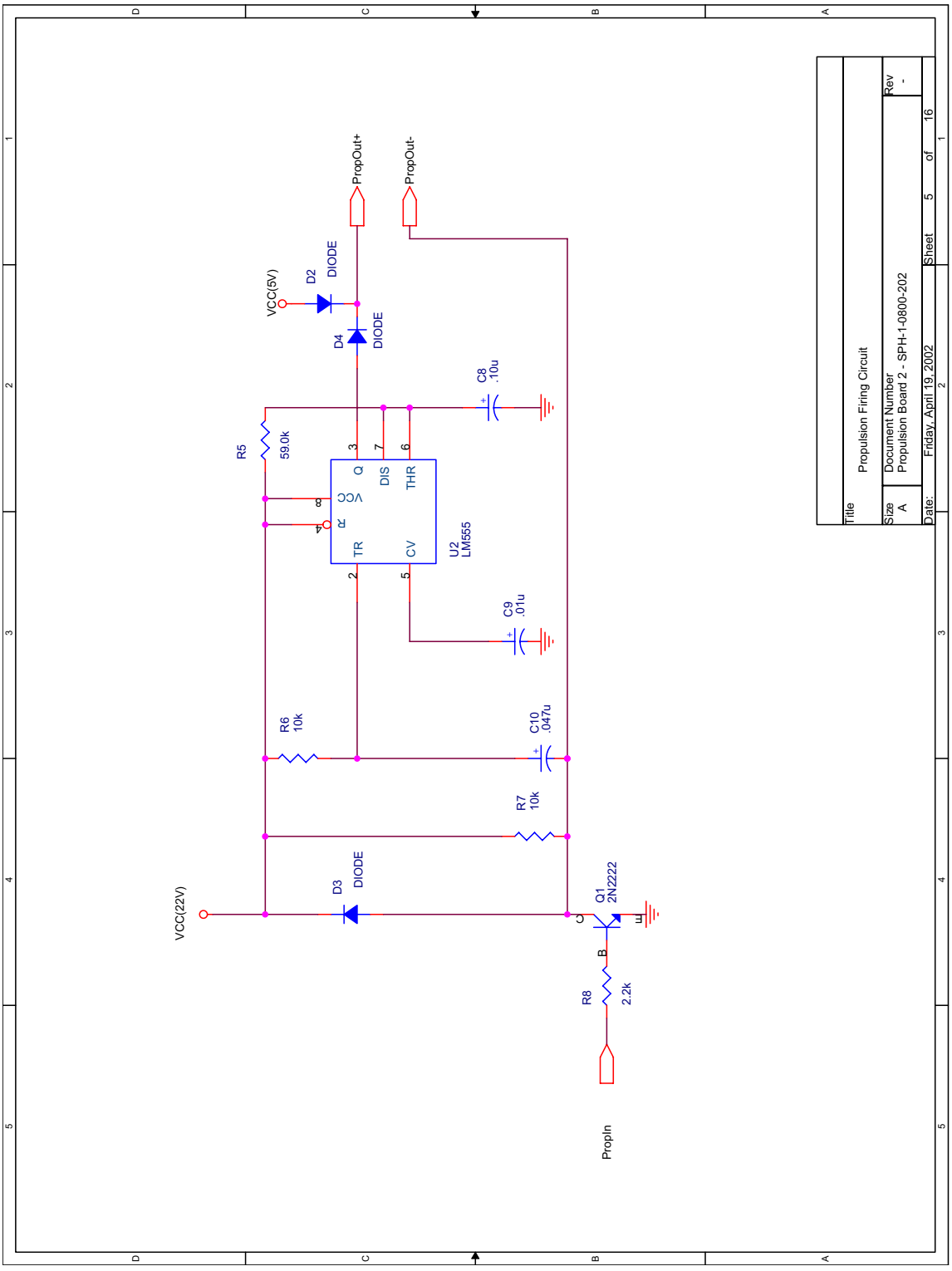
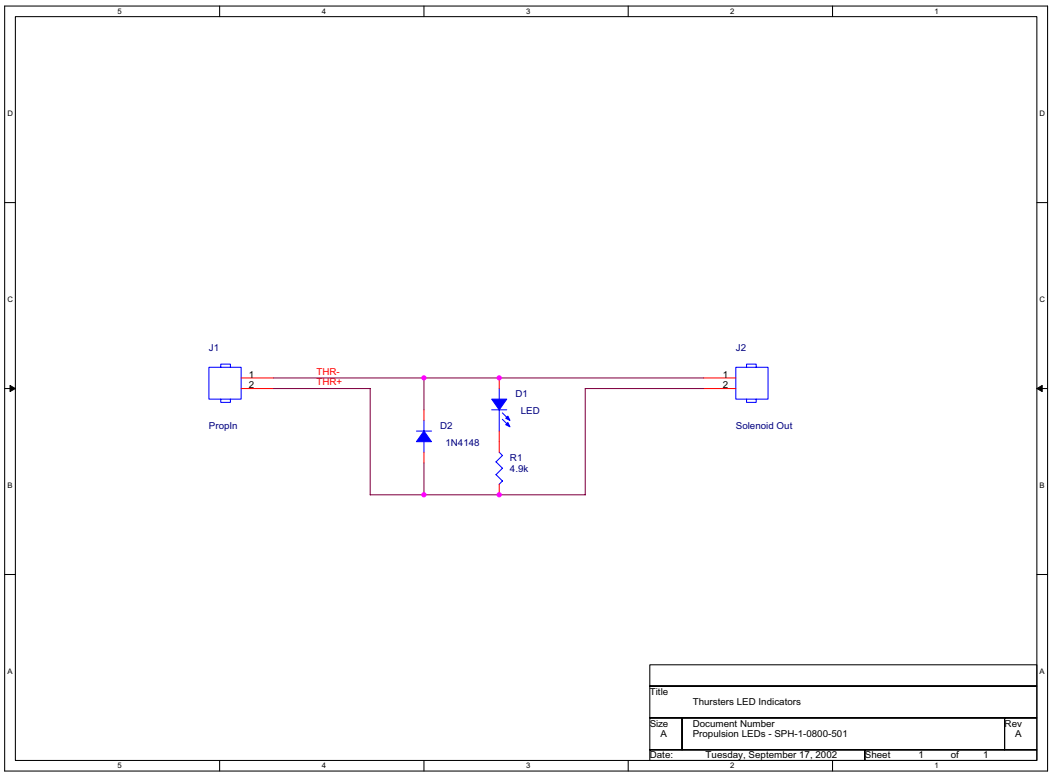
16

The following schematic repeats twelve times, once per signal/solenoid:






## F.1.3 Data Processing (C6701 DSP / SMT375)

### Design Drivers

- Support other subsystems' data processing needs
  - Communications data processing
  - Metrology computational support
  - Propulsion thruster actuation
  - Provide house-keeping information to user
    - Battery information
    - Tank usage
- Allow reconfiguration of control algorithms
  - Enable the complete software to be changed to allow testing of programs with different configurations and goals
- Maximize processing power for available volume and power

- Minimize processing needs of ‘bus’ system to maximize processing power available for control algorithms

**Functional Block Diagram**

A COTS product was selected to perform the data processing within each SPHERES satellite. The selected product is a Sundance Multiprocessor Technology Ltd SMT375 board which features a Texas Instruments TMS320C6701 Digital Signal Processor (DSP). The SMT375 board utilizes the Texas Instruments Module standard for the C40 DSP (TIM40), used in the prototype design of SPHERES. The standard implements a 32 bit global data bus with 31 address lines, plus six TI communications ports which split 32 bit data into bytes for a maximum data speed of 20MBps. A block diagram (simplified from [Sundance, 2003]) of the SMT375 board is presented in Figure F.6. The SPHERES metrology FPGA interfaces via the global data bus, while the communications system utilizes the commports.The features of the SMT375 board are summarized in Table F.8

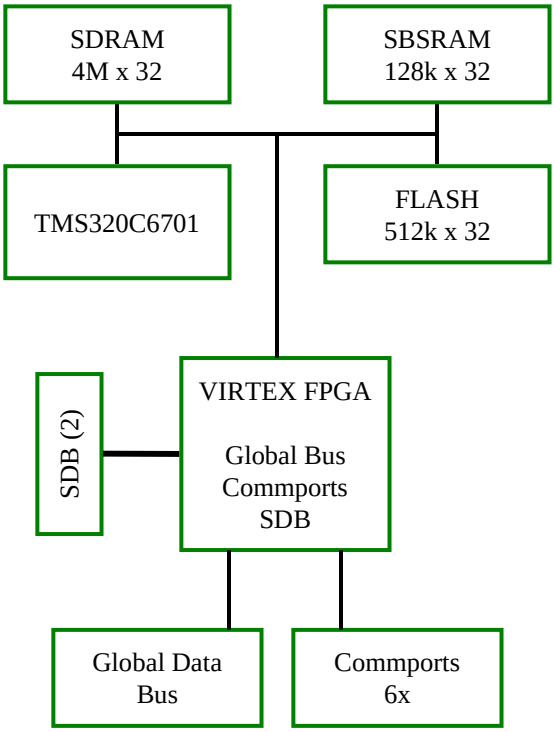



**Figure F.6** SMT375 functional block diagram

**TABLE F.8** Features of the SMT375 board

| | |
|---|---|
| **Form Factor** | Single-width TIM40 |
| **CPU** | TMS320C6701 |
| **Speed** | 167MHz |
| **FLOPS** | 1 GFLOPS peak |
| **RAM** | 16MB (4M x 32) |
| **Cache** | 512k (128k x 32) |
| **Commports** | 6 x 20MBps |
| **Programming** | C and C++ |
| **Power Consumption** | 7 W |

The SMT375 interfaces to the rest of the sub-systems through the metrology FPGA board via three 80-pin connectors. The signal descriptions of these connectors are explained in the metrology and communications sections which utilize them.

## F.1.4 Metrology

**Design Drivers**

- Provide real-time position and attitude information of each satellite
- Implements measurement circuitry for metrology
  - One infrared transmitter command (protected)
  - 12 infrared receiver channels
  - 24 ultrasound receiver channels
  - Six 12-bit A/D channels, up to 1KHz
- Propulsion register (to control solenoid valves)
  - 12 outputs with read-back capability
- General output register
  - Two outputs with read-back capability
- General input register
  - Two inputs

### Functional Block Diagrams

Because the metrology motherboard is the only board which interfaces directly with the SMT375 DSP board, it functions not only to support metrology, but also to provide general input/output signals and pass-through of the commports and power to the communications system. To implement these functions the metrology system centers its design around an FPGA as pictured in Figure F.7. The system interfaces to the twelve US/IR boards, the internal beacon, three gyroscopes, and three accelerometers (with amplifiers). An EEPROM stores the configuration of the FPGA and interfaces to a JTAG port to update the programming as necessary.

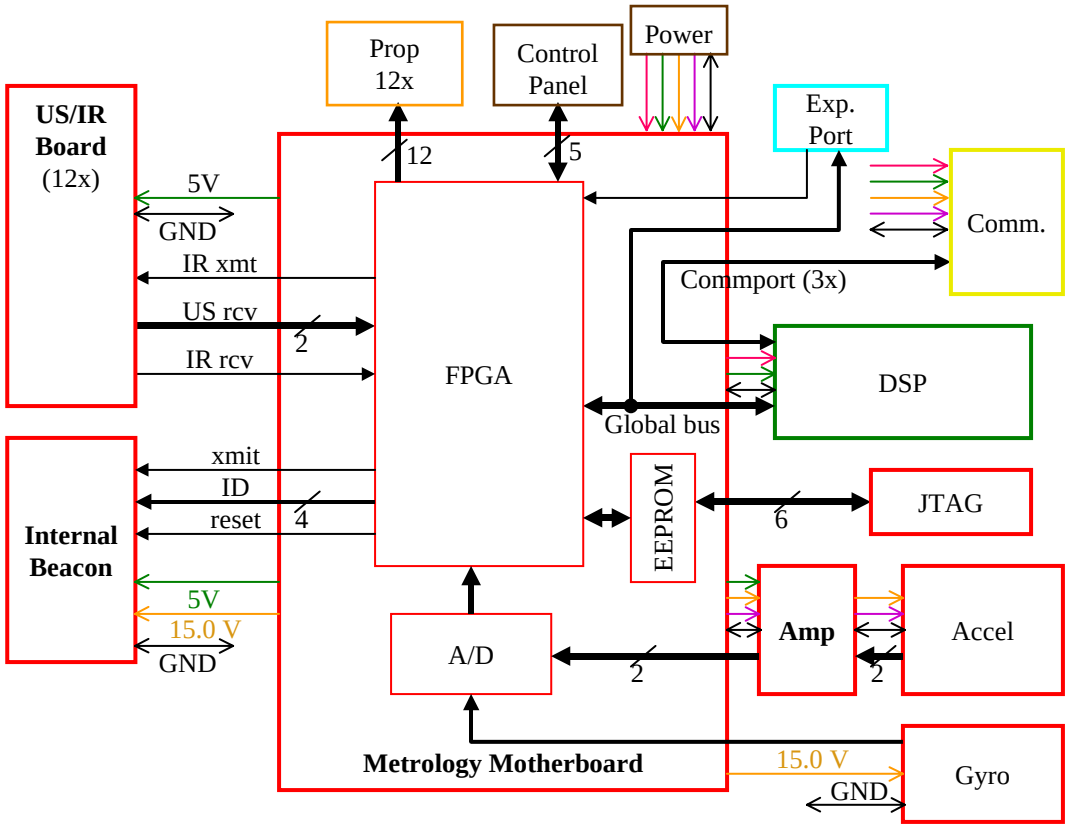



**Figure F.7** Metrology sub-system functional block diagram

The four boards that support the metrology sub-system (motherboard, US/IR, accelerometer amplifier, and internal beacon) are described next.

### Metrology Motherboard

The metrology system utilizes a Xilinx FPGA which interfaces with the DSP via the global bus and implements general input/output for the propulsion and control panel boards. The FPGA also collects the range measurements of the US/IR system independently of the DSP, to minimize the load of the metrology system on the DSP. The FPGA implements its own 25MHz counter which is reset automatically when an IR signal is received; registers on the FPGA store the time taken to receive an ultrasound signal at each of the 24 receivers without interrupting the DSP. The DSP is only interrupted once after each beacon transmits its signal (i.e., a total of five times when five beacons are in use, but not 120 times if each receiver interrupted). The parallel processing of the FPGA ensures that the signals from each receiver are recorded correctly. The FPGA interfaces with a 12-bit analog to digital converter to provide up to 1kHz data from the gyroscopes and accelerometers. The board provides a single pole low-pass filter with a drop-off frequency at 300Hz implemented with a simple RC circuit. Because the metrology motherboard is oriented in the X plane, it hosts one accelerometer and its amplification circuit. Figure F.8 shows a schematic of the FPGA firmware design.

Table F.9 describes the inputs and outputs of the metrology mother board.

**TABLE F.9** Metrology motherboard signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *From Power* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+3.3V) | Pwr | +3.3V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |

**TABLE F.9** Metrology motherboard signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Data to power and propulsion stack* | THR 1-12 | Out | Pass through signals for thrusters 1-12 |
| | /Enable | In | Enable button signal |
| | /LED-enable | Out | Enable LED signal |
| | /Batlow | In | Low battery indicator signal |
| | WDOG | Out | Watchdog control signal |
| | /RESET | In | Reset |
| *Data and power to SMT375* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+3.3V) | Pwr | +3.3V power |
| | GND | Pwr | Common ground |
| | C[0-5] D[0-7] | I/O | Commport data lines |
| | CACK[0-5] | I/O | Commport acknowledge signal |
| | CRDY[0-5] | I/O | Commport ready signal |
| | CREQ[0-5] | I/O | Commport request signal |
| | STRB[0-5] | I/O | Commport strobe |
| | /RESET | Out | Reset Line |
| | IR_RCV_INT | Out | Infrared reception interrupt. It is asserted when an IR is received so the DSP can prepare for a global metrology cycle |
| | PADS_INT | Out | 1kHz interrupt. Provides timing for the DSP and indicates IMU data is available. |
| | A0-A30 | Out | Global bus address lines |
| | D0-D31 | I/O | Global bus data lines |
| | RDY1 | Out | Global bus ready |
| | PAGE1 | In | Global bus page select |
| | STRB1 | In | Global bus strobe |
| | R/W1 | In | Global bus read/write |
| | /CE1 | Out | Global bus control lines enable |
| | /OE | Out | Global bus data lines enable |
| | /AE | Out | Global bus address lines enable |

**TABLE F.9** Metrology motherboard signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Data and power to communications board* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+3.3V) | Pwr | +3.3V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |
| | A0-A30 | Out | Global bus address lines (expansion port) |
| | D0-D31 | I/O | Global bus data lines (expansion port) |
| | RDY1 | I/O | Global bus ready (expansion port) |
| | PAGE1 | I/O | Global bus page select (expansion port) |
| | STRB1 | Out | Global bus strobe (expansion port) |
| | R/W1 | I/O | Global bus read/write (expansion port) |
| | /RESET | Out | Reset line |
| | /Exp_port_in | In | High when an expansion port selects to bypass the satellite US/IR metrology boards |
| | IR_XMIT | Out | IR transmit command |
| | US-RX[11-12]-[1-2] | In | Input ultrasound signals from the expansion port board |
| | IR-RX[11-12] | In | Input infrared signals from the expansion port board |
| | EXP A2D [0-2] | In | Input analog signals from the expansion port board |
| | C[1,2,4] D[0-7] | I/O | Commport data lines |
| | CACK[1,2,4] | I/O | Commport acknowledge signal |
| | CRDY[1,2,4] | I/O | Commport ready signal |
| | CREQ[1,2,4] | I/O | Commport request signal |
| | STRB[1,2,4] | I/O | Commport strobe |
| *US/IR Boards (12x)* | Vcc(+5V) | Pwr | +5V power |
| | GND | Pwr | Common ground |
| | IR_XMIT | Out | IR transmit command |
| | US-RX[1-2] | In | Input ultrasound signals |
| | IR-RX | In | Input infrared signal |

**TABLE F.9** Metrology motherboard signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Onboard beacon* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+15V) | Pwr | +15V power |
| | GND | Pwr | Common ground |
| | IR_RCV_INT | Out | IR Received interrupt signal - commands the beacon to initiate its US transmit process |
| | B-MCLR | Out | Beacon enable/reset |
| | B-NUM[0-3] | Out | Beacon configuration number |
| *Gyros. (3x)* | Vcc(+15V) | Pwr | +15V power |
| | GND | Pwr | Common ground |
| | [X,Y,Z] Gyro | In | Gyroscope analog signal |
| *Accels. (2x)* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |
| | [Y,Z] Accel-Amp | In | Y and Z accelerometer amplified analog signals |
| | [Y,Z] Temp-Temp | In | Y and Z accelerometer temperature sensor signal |
| *JTAG* | Vcc(+3.3V) | Pwr | +3.3V power |
| | GND | Pwr | Common ground |
| | PTCK | In | Clock |
| | PTDO | Out | Data out |
| | PTDI | In | Data in |
| | PTMS | In | Select |

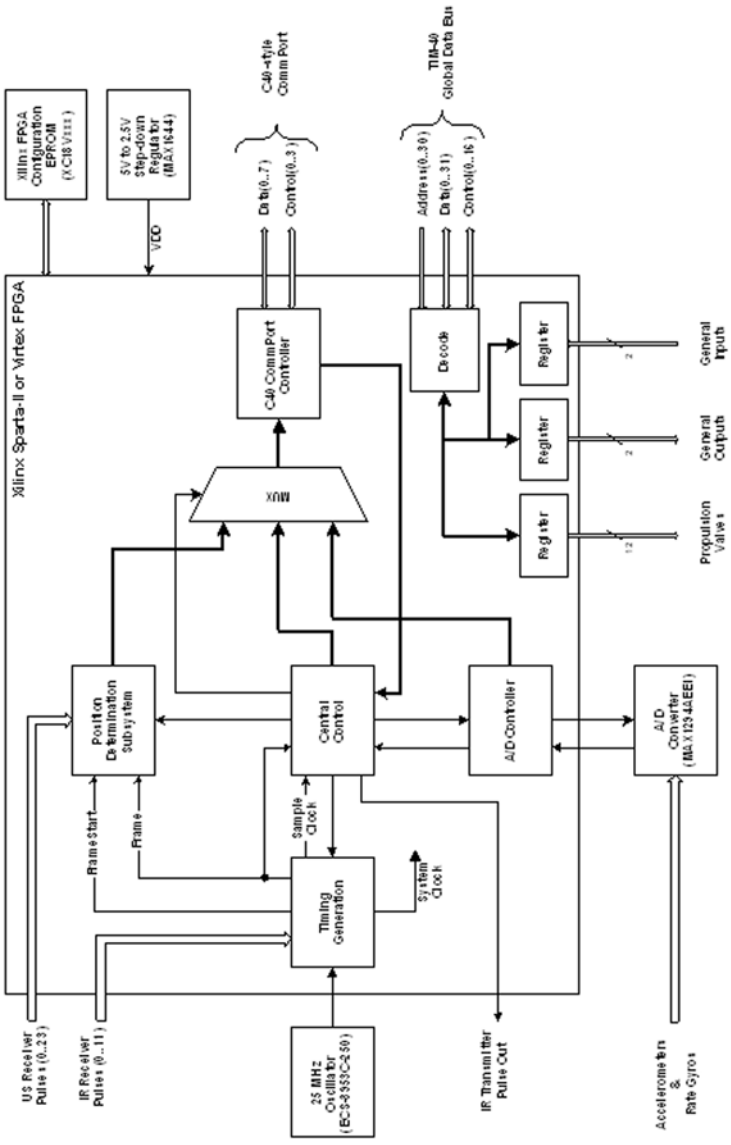



**Figure F.8** FPGA firmware design

## Metrology US/IR Boards

The metrology ultrasound/infrared board receive and amplify the ultrasound signals emitted by the global metrology beacons. They also transmit and receive the infrared signal which initiates the global metrology process. Therefore, as pictured in Figure F.9, each board consists of three main elements: infrared transmit, infrared receive, and ultrasound receive. The infrared transmit circuit uses a transistor to drive 1A of current through an

infrared LED; the FPGA ensures the 1A pulse is no longer than 10μs and has a maximum duty cycle of 10% to protect the LEDs. The infrared receive utilizes a COTS receiver which directly outputs a logic signal to the FPGA. The ultrasound receive signal required the use of a quad op-amp to amplify, rectify, and digitize the signal. A schematic of the circuit is presented in Figure F.10. The signals of the US/IR boards are described in Table F.9, reversing inputs and outputs.

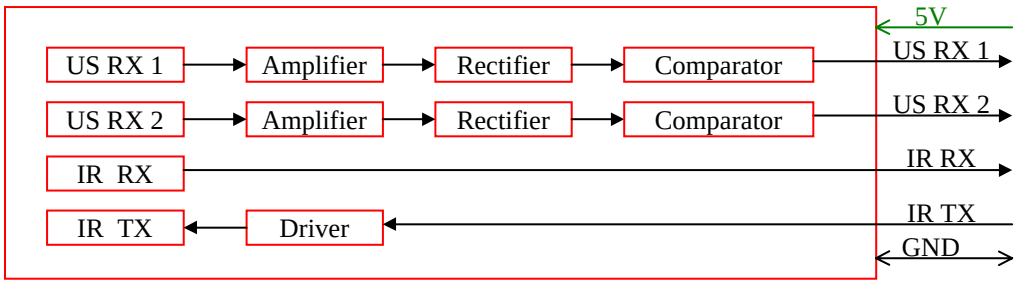



**Figure F.9** US/IR boards functional block diagram

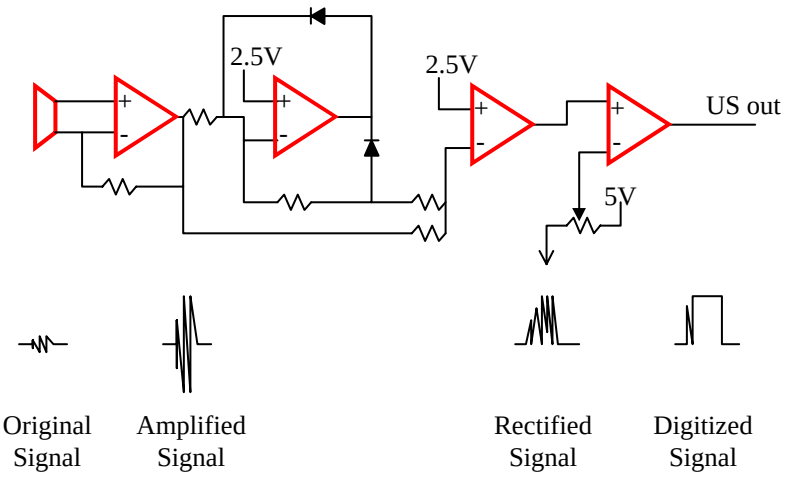



**Figure F.10** Ultrasound amplification schematic

### Accelerometer Amplifier Boards

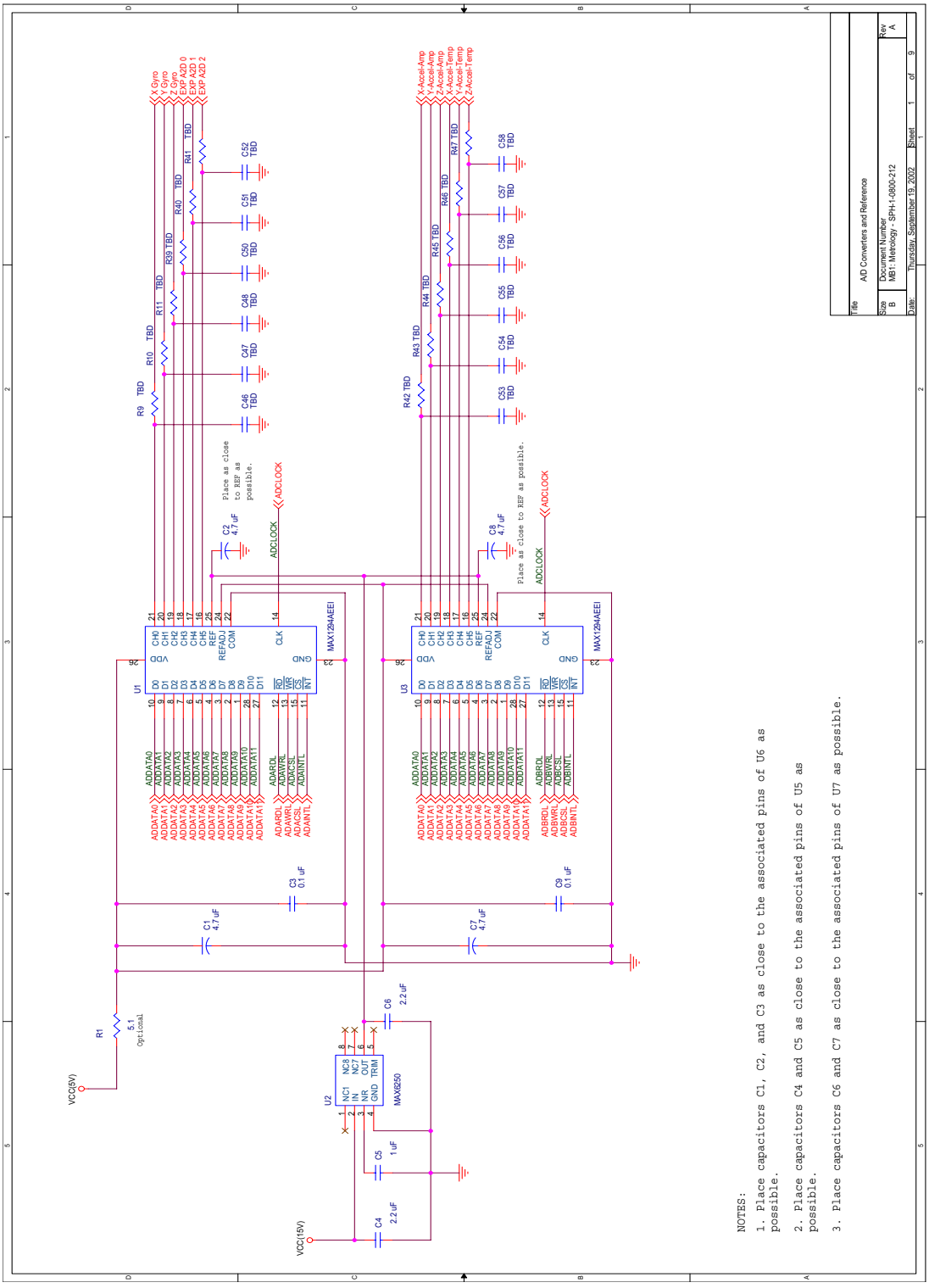
The selected accelerometers have an operational range of ±30g but are capable of measuring accelerations with milli-g precision. Because the SPHERES thrusters create accelerations in the milli-g range, the accelerometer require custom amplifiers to provide the necessary 0-5V analog signal required by the A2D converter. The accelerometer operate like current sources, therefore they require a sense resistor at the output to create a voltage for measurement. The circuit selected a sense resistor which allows the use of a high-frequency op-amp to amplify the input signal 40 times. The accelerometers also output a temperature measurement signal from a thermistor, so that software can take into account temperature changes. While not used in the initial implementation of SPHERES, the accelerometer boards send the temperature signal to the FPGA in case it proves necessary in the future. A description of the signals of the accelerometer boards is presented in Table F.9, reversing inputs and outputs.

### Internal Beacon

The internal beacon replicates an external beacon (see Section F.3 below), but omits the infrared reception circuitry, does not use a manual switch, and utilizes custom power regulation circuitry. The infrared circuitry and ID number selector are replaced by signals from the FPGA. The power sub-system provides regulated 5V. The internal beacon regulates +15V to +12V using a linear regulator. Descriptions of the signals are presented in Table F.9, reversing inputs and outputs.

### Schematics

The schematics for all the metrology boards are presented next.


NOTES:
1. Place capacitors C1, C2, and C3 as close to the associated pins of U6 as possible.
2. Place capacitors C4 and C5 as close to the associated pins of U5 as possible.
3. Place capacitors C6 and C7 as close to the associated pins of U7 as possible.
A/D Converters and Reference
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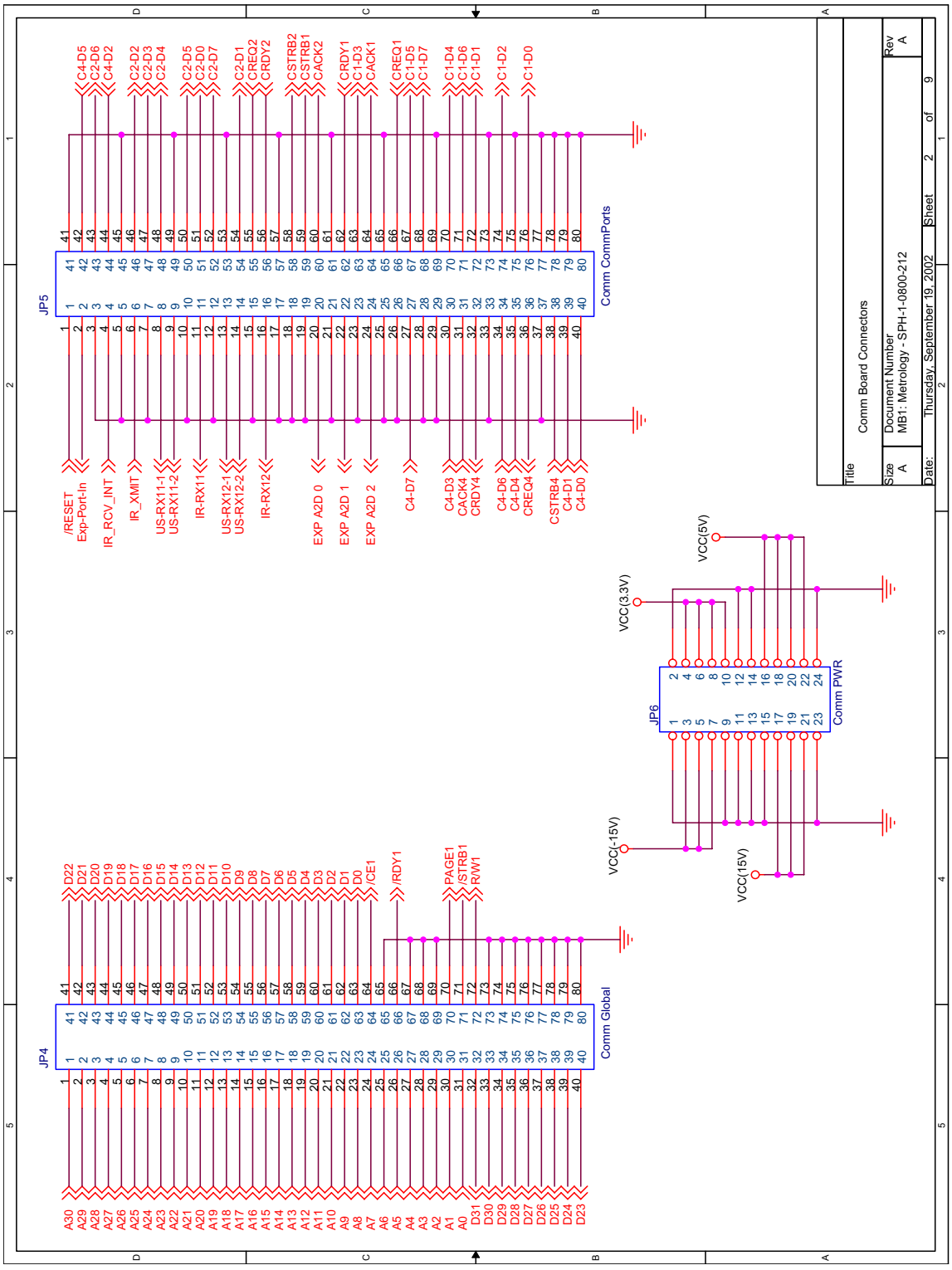
Thursday, September 19, 2002
MAX1294AEEI
MAX6250
ADCLOCK
VCC(5V)
VCC(15V)


JP4
Comm Global
JP5
Comm CommPorts
JP6
Comm PWR
/RESET
Exp-Port-In
IR_RCV_INT
IR_XMIT
US-RX11-1
US-RX11-2
IR-RX11
US-RX12-1
US-RX12-2
IR-RX12
EXP A2D 0
EXP A2D 1
EXP A2D 2
C4-D7
C4-D3
CACK4
CRDY4
C4-D6
C4-D4
CREQ4
CSTRB4
C4-D1
C4-D0
/RDY1
PAGE1
/STRB1
R/W1
/CE1
VCC(-15V)
VCC(3.3V)
VCC(5V)
VCC(15V)
Title
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Size
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Date:
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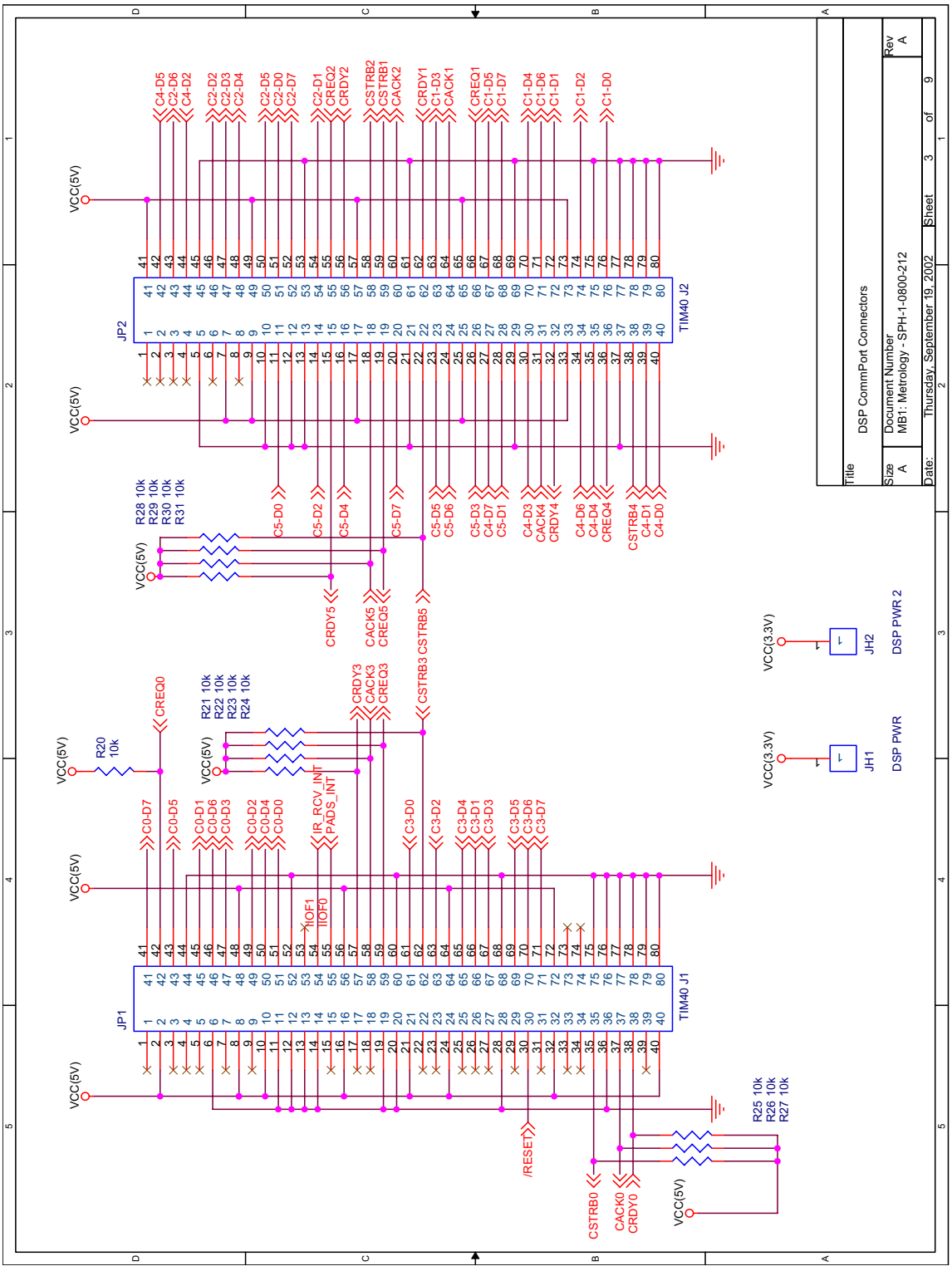
9


JP1
TIM40 J1
JP2
TIM40 J2
JH1
DSP PWR
JH2
DSP PWR 2
VCC(5V)
VCC(3.3V)
R20 10k
R21 10k
R22 10k
R23 10k
R24 10k
R25 10k
R26 10k
R27 10k
R28 10k
R29 10k
R30 10k
R31 10k
/RESET
IR_RCV_INT
PADS_INT
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Size A
Document Number MB1: Metrology - SPH-1-0800-212
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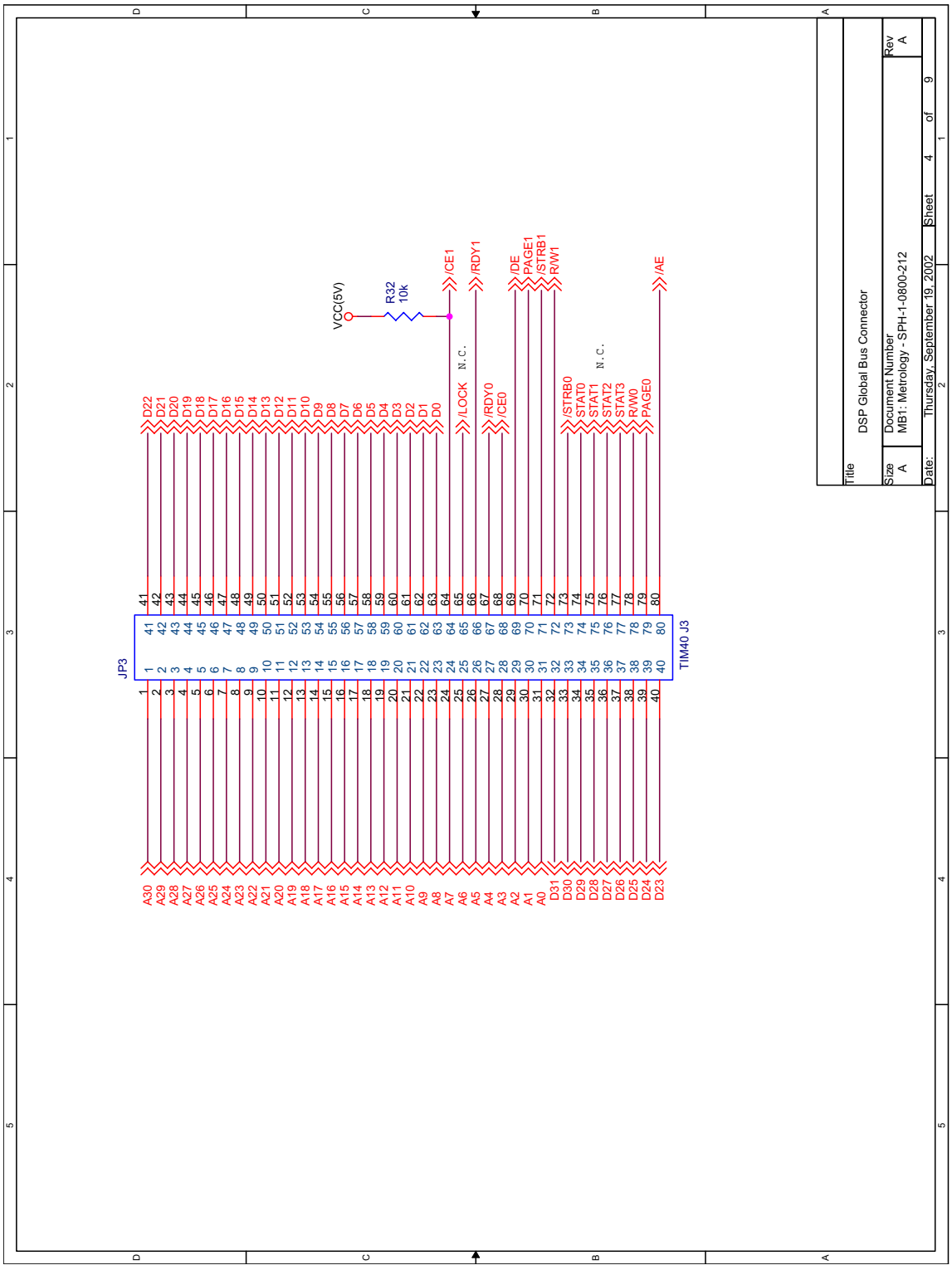
JP3
TIM40 J3
VCC(5V)
R32
10k
/CE1
/RDY1
/IDE
PAGE1
/STRB1
R/W1
/AE
N.C.
/LOCK
/RDY0
/CE0
/STRB0
STAT0
STAT1
STAT2
STAT3
R/W0
PAGE0
N.C.
D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
A30 A29 A28 A27 A26 A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 D31 D30 D29 D28 D27 D26 D25 D24 D23
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Size A
Document Number
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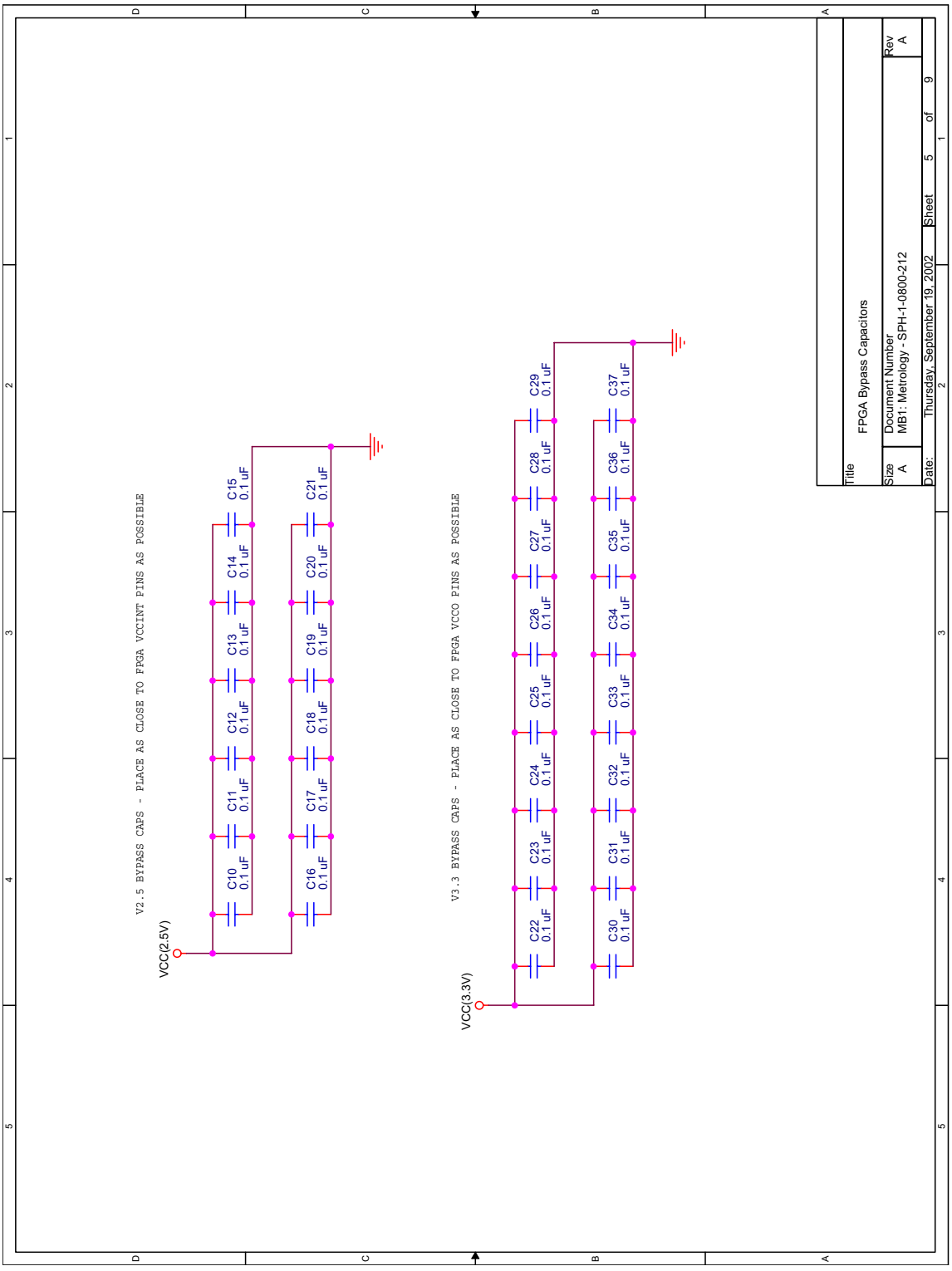
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VCC(2.5V)
C10 0.1 uF
C11 0.1 uF
C12 0.1 uF
C13 0.1 uF
C14 0.1 uF
C15 0.1 uF
C16 0.1 uF
C17 0.1 uF
C18 0.1 uF
C19 0.1 uF
C20 0.1 uF
C21 0.1 uF
V3.3 BYPASS CAPS - PLACE AS CLOSE TO FPGA VCCO PINS AS POSSIBLE
VCC(3.3V)
C22 0.1 uF
C23 0.1 uF
C24 0.1 uF
C25 0.1 uF
C26 0.1 uF
C27 0.1 uF
C28 0.1 uF
C29 0.1 uF
C30 0.1 uF
C31 0.1 uF
C32 0.1 uF
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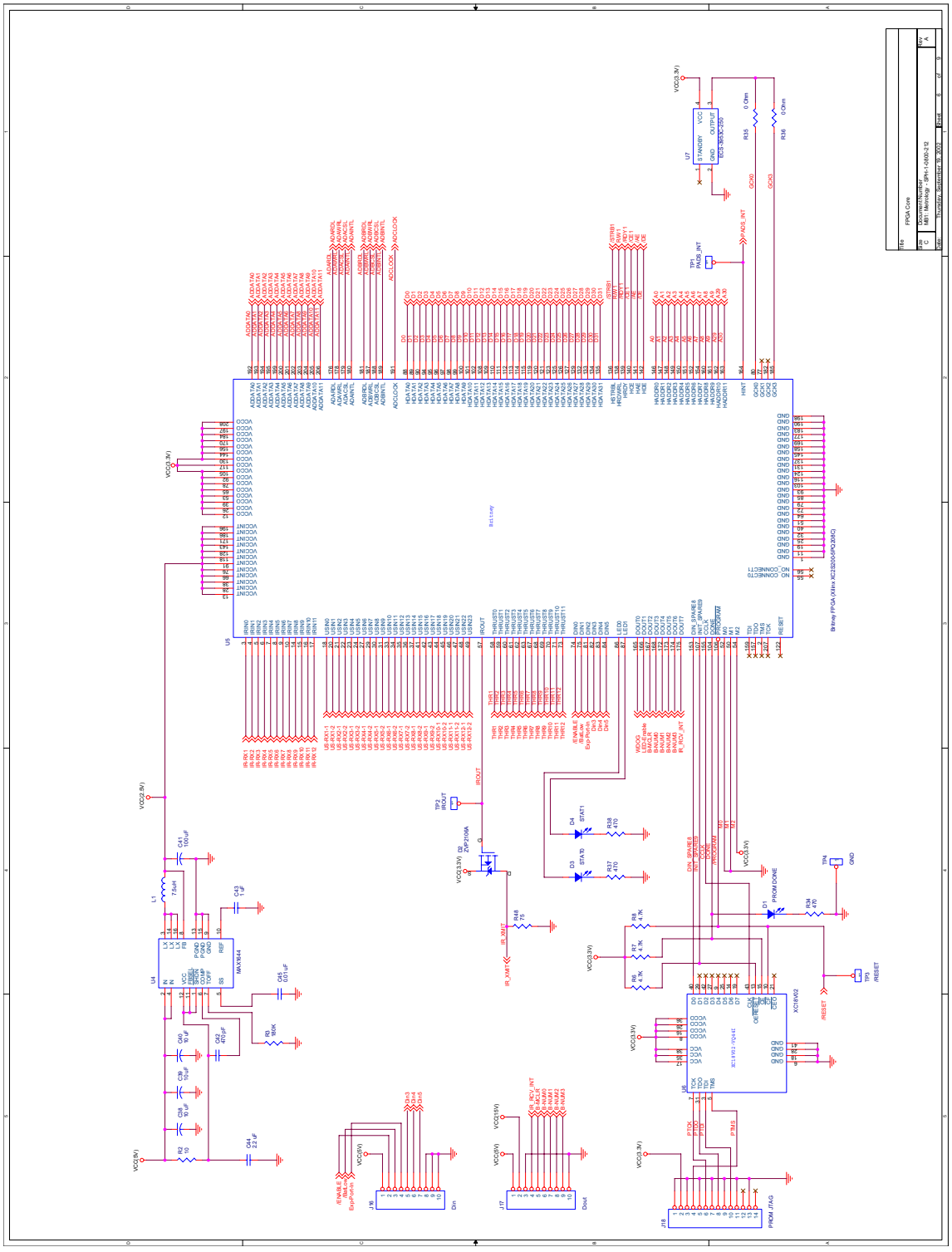

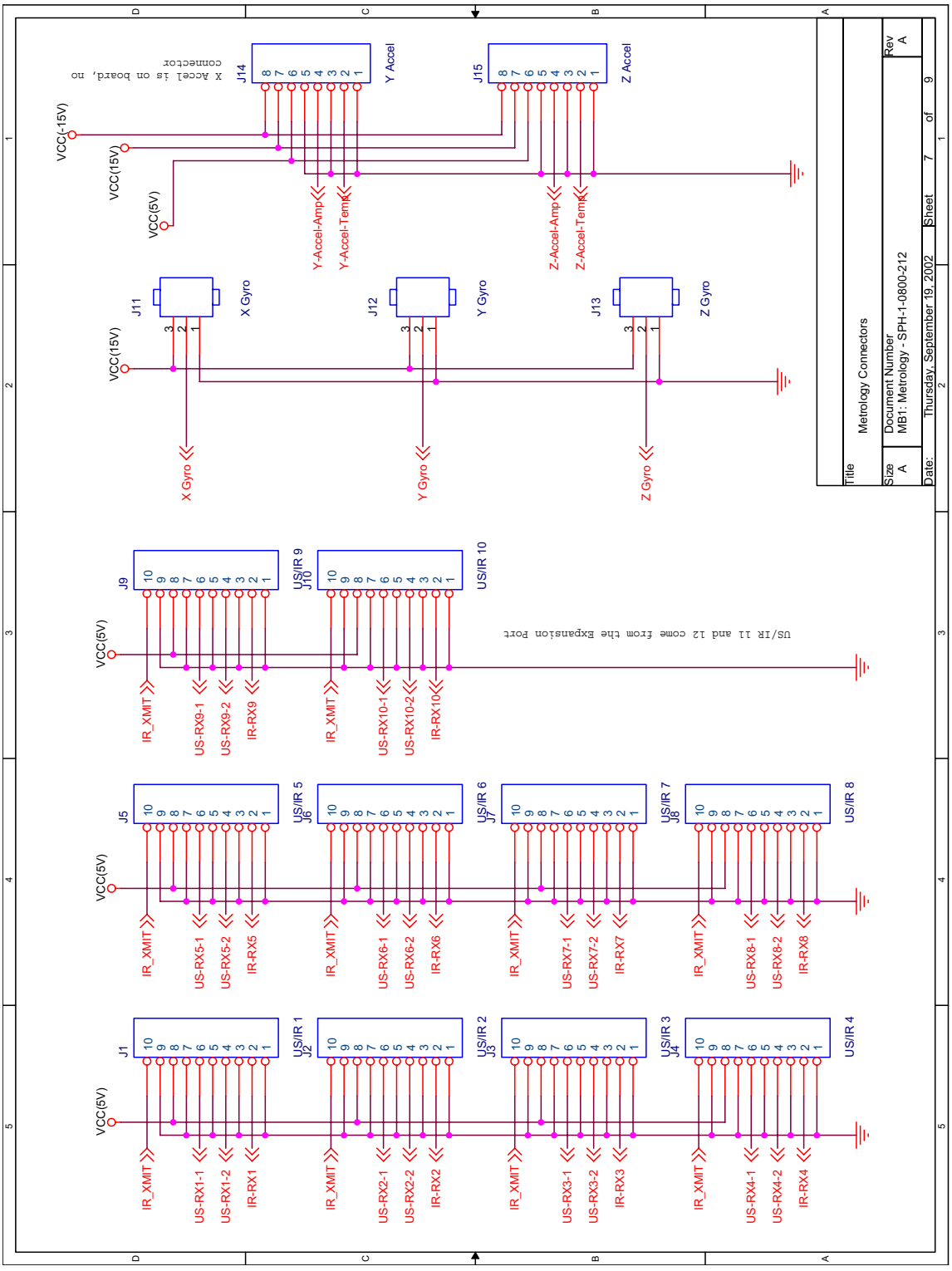
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J14
Y Accel
J15
Z Accel
VCC(-15V)
VCC(15V)
VCC(5V)
Y-Accel-Amp
Y-Accel-Temp
Z-Accel-Amp
Z-Accel-Temp
J11
X Gyro
J12
Y Gyro
J13
Z Gyro
US/IR 9
US/IR 10
US/IR 5
US/IR 6
US/IR 7
US/IR 8
US/IR 1
US/IR 2
US/IR 3
US/IR 4
IR_XMIT
US-RX9-1
US-RX9-2
IR-RX9
US-RX10-1
US-RX10-2
IR-RX10
US-RX5-1
US-RX5-2
IR-RX5
US-RX6-1
US-RX6-2
IR-RX6
US-RX7-1
US-RX7-2
IR-RX7
US-RX8-1
US-RX8-2
IR-RX8
US-RX1-1
US-RX1-2
IR-RX1
US-RX2-1
US-RX2-2
IR-RX2
US-RX3-1
US-RX3-2
IR-RX3
US-RX4-1
US-RX4-2
IR-RX4
US/IR 11 and 12 come from the Expansion Port
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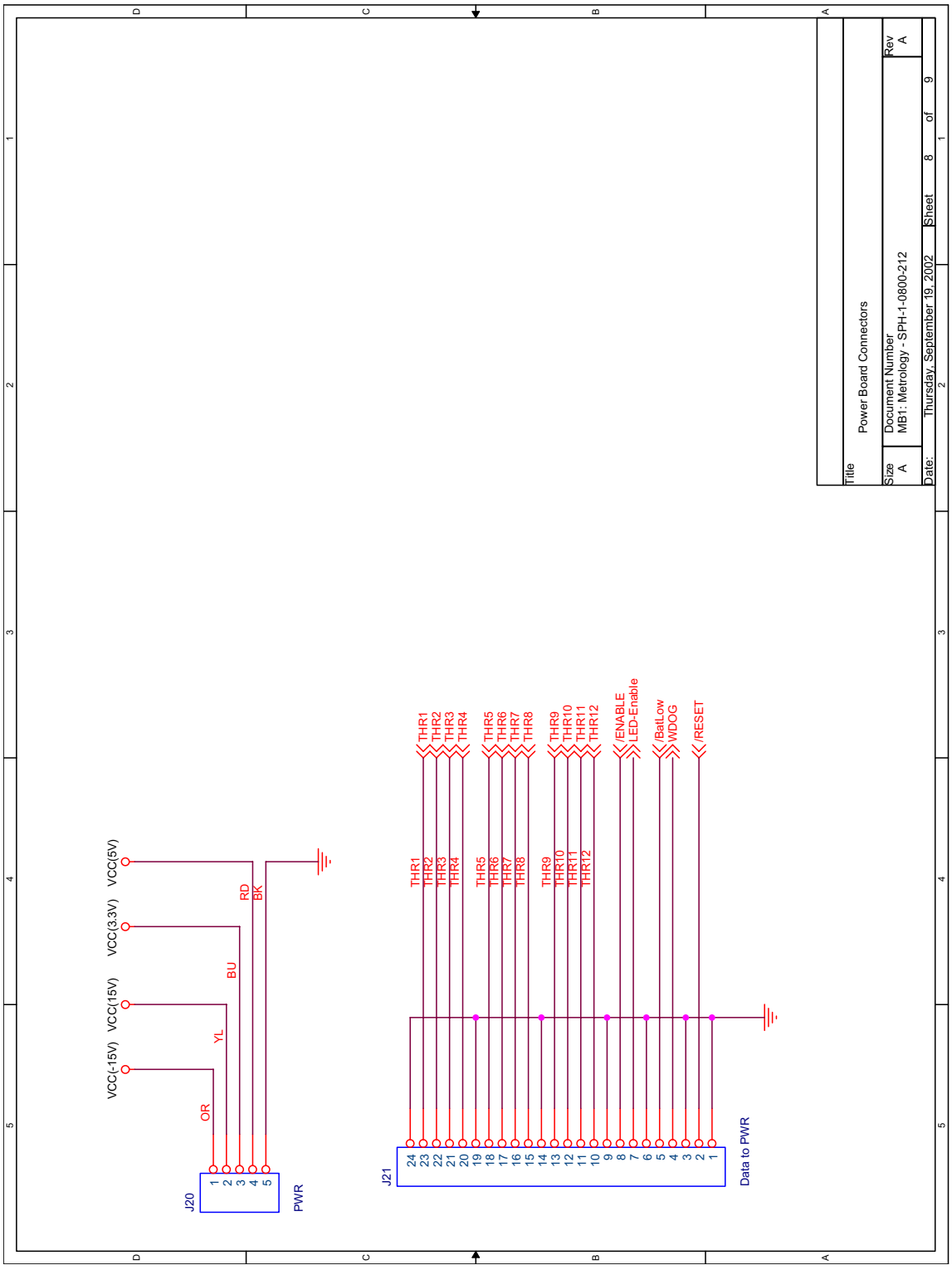
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Size
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Document Number
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Rev
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Thursday, September 19, 2002
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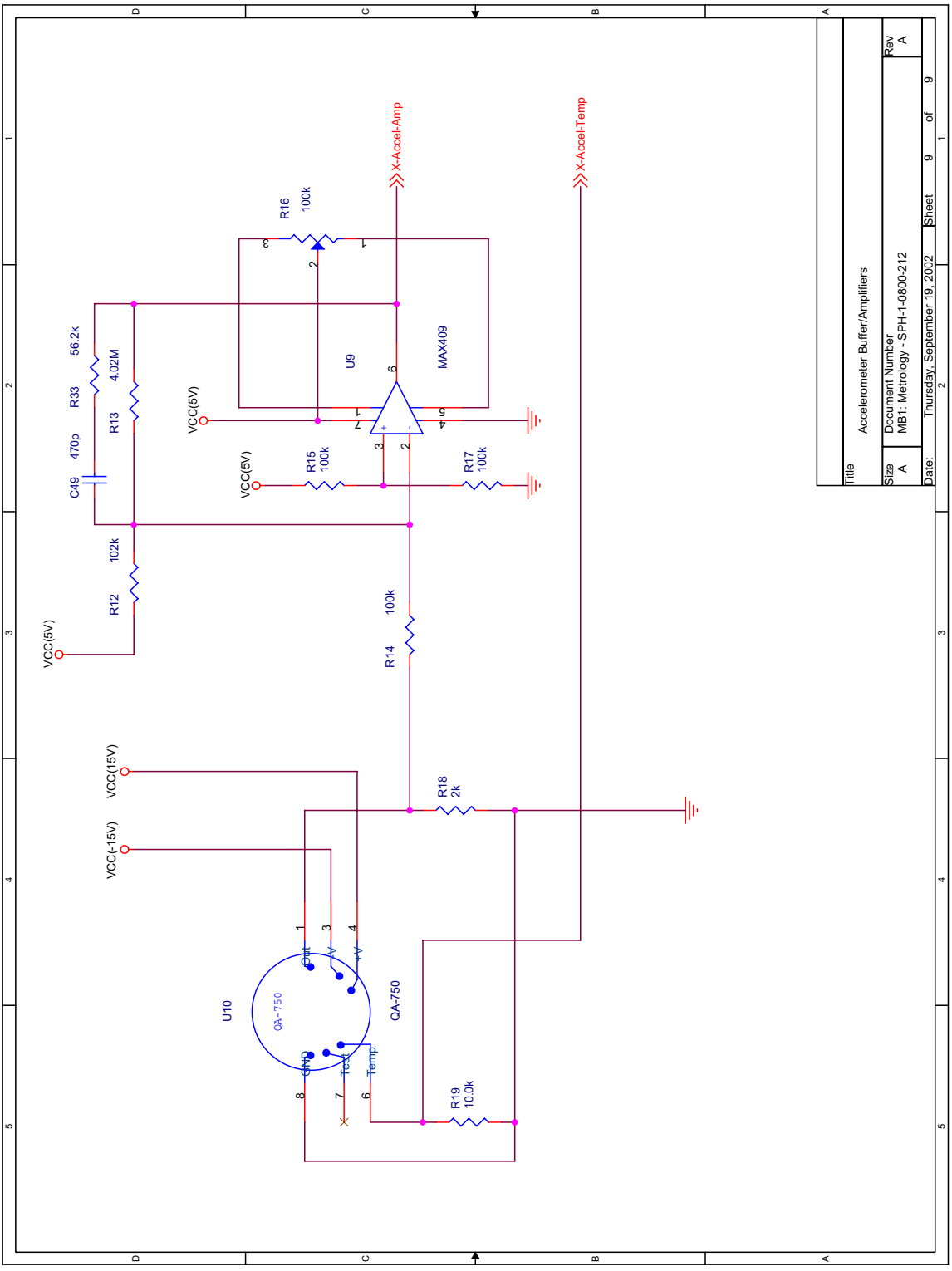
8
of
9
VCC(5V)
VCC(3.3V)
VCC(15V)
VCC(-15V)
RD
BK
BU
YL
OR
J20
PWR
THR1
THR2
THR3
THR4
THR5
THR6
THR7
THR8
THR9
THR10
THR11
THR12
/ENABLE
LED-Enable
/BatLow
WDOG
/RESET
J21
Data to PWR


X-Accel-Amp
X-Accel-Temp
R16 100k
U9
MAX409
R33 56.2k
R13 4.02M
C49 470p
R12 102k
R14 100k
R15 100k
R17 100k
R18 2k
R19 10.0k
U10
QA-750
VCC(5V)
VCC(15V)
VCC(-15V)
Out
-V
+V
GND
Test
Temp
Title
Accelerometer Buffer/Amplifiers
Size A
Document Number MB1: Metrology - SPH-1-0800-212
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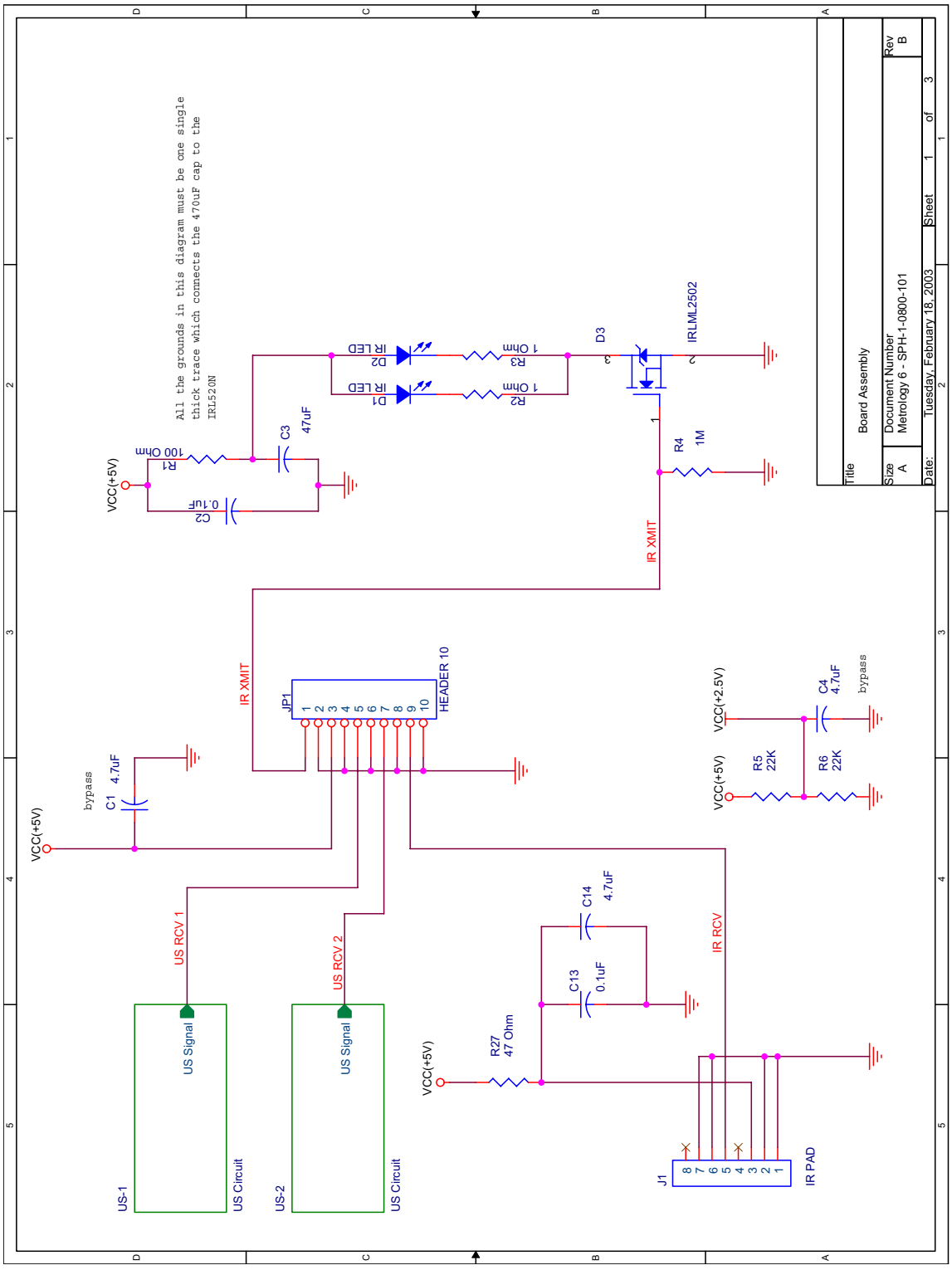
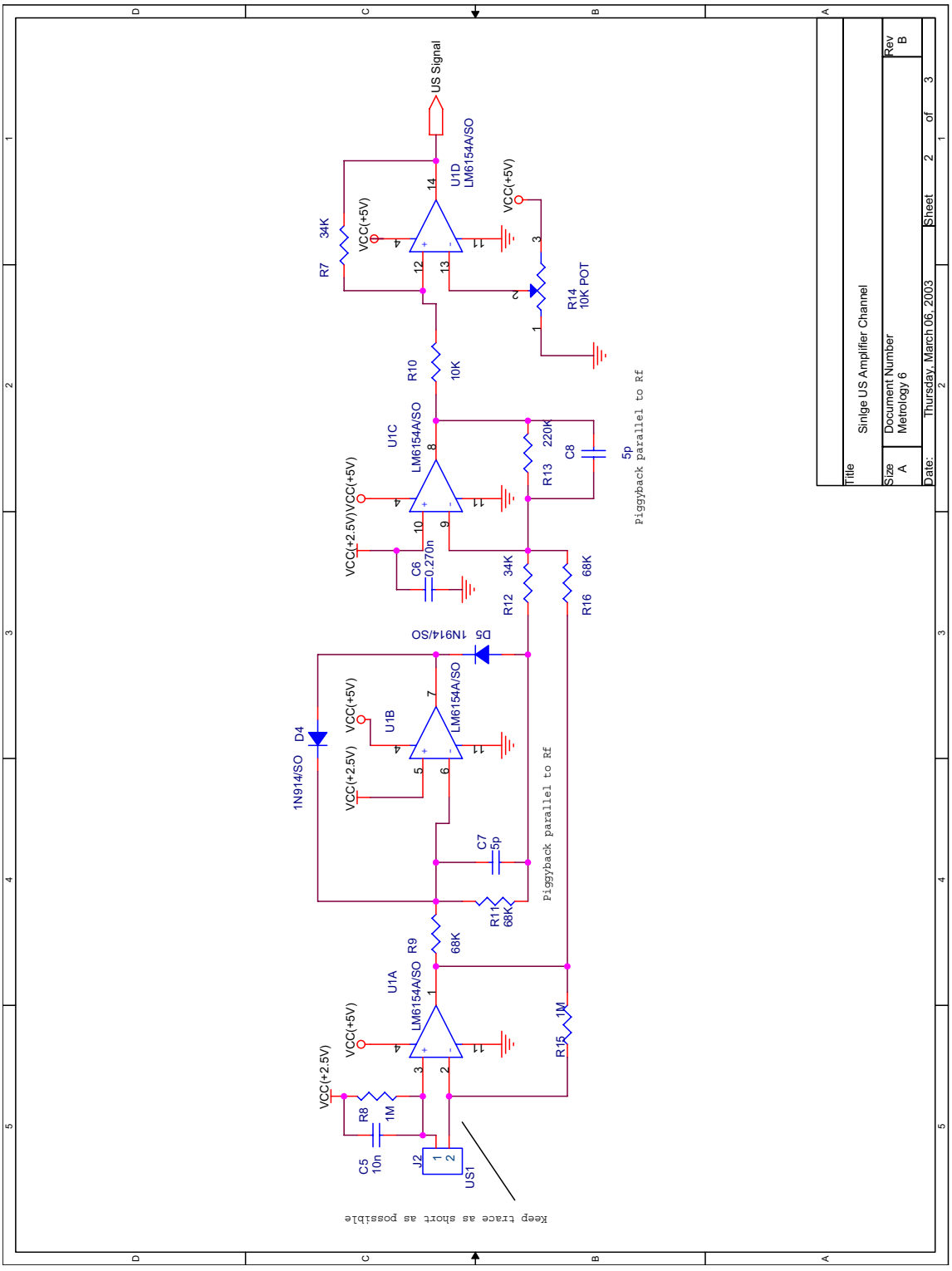
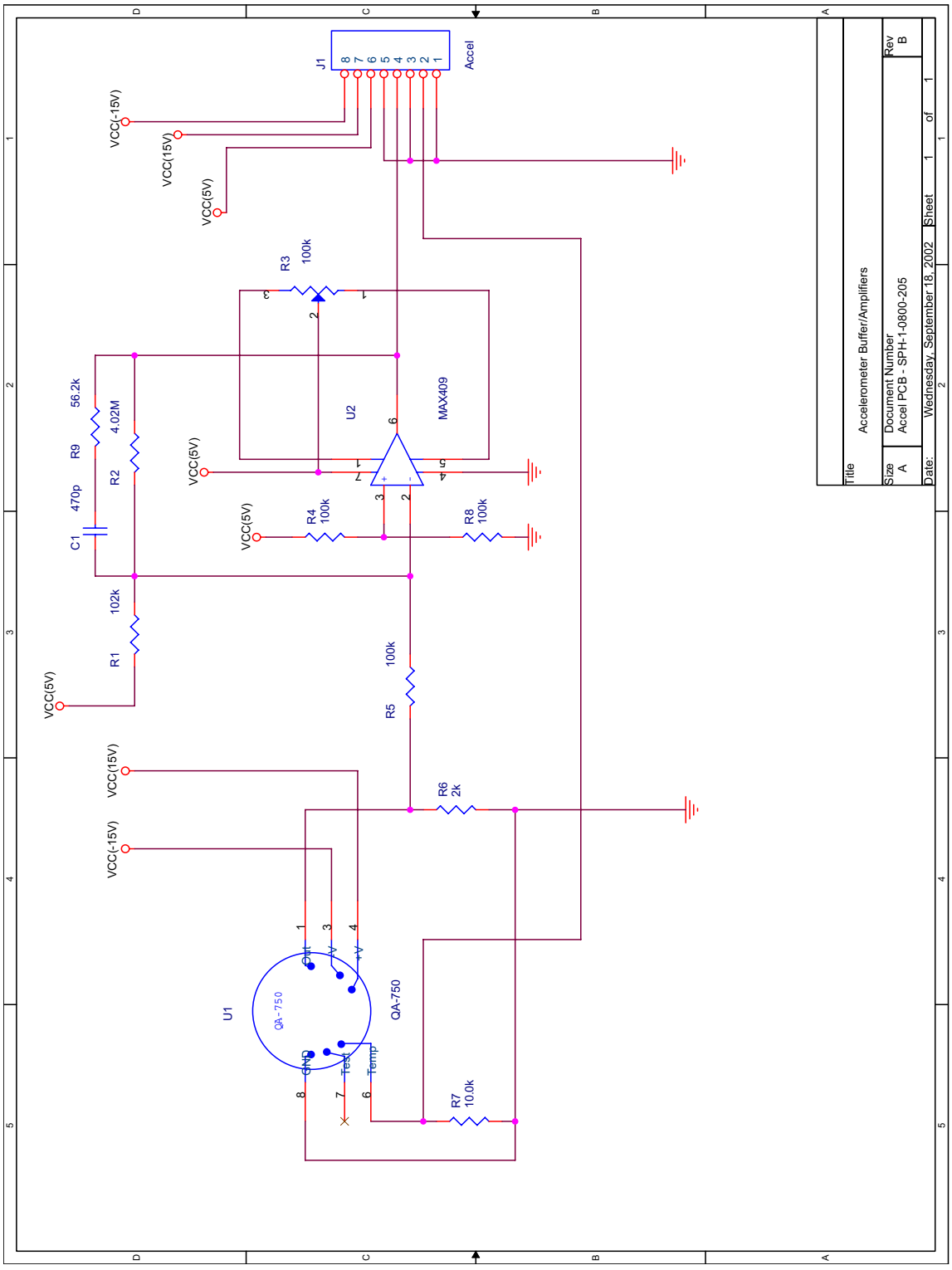
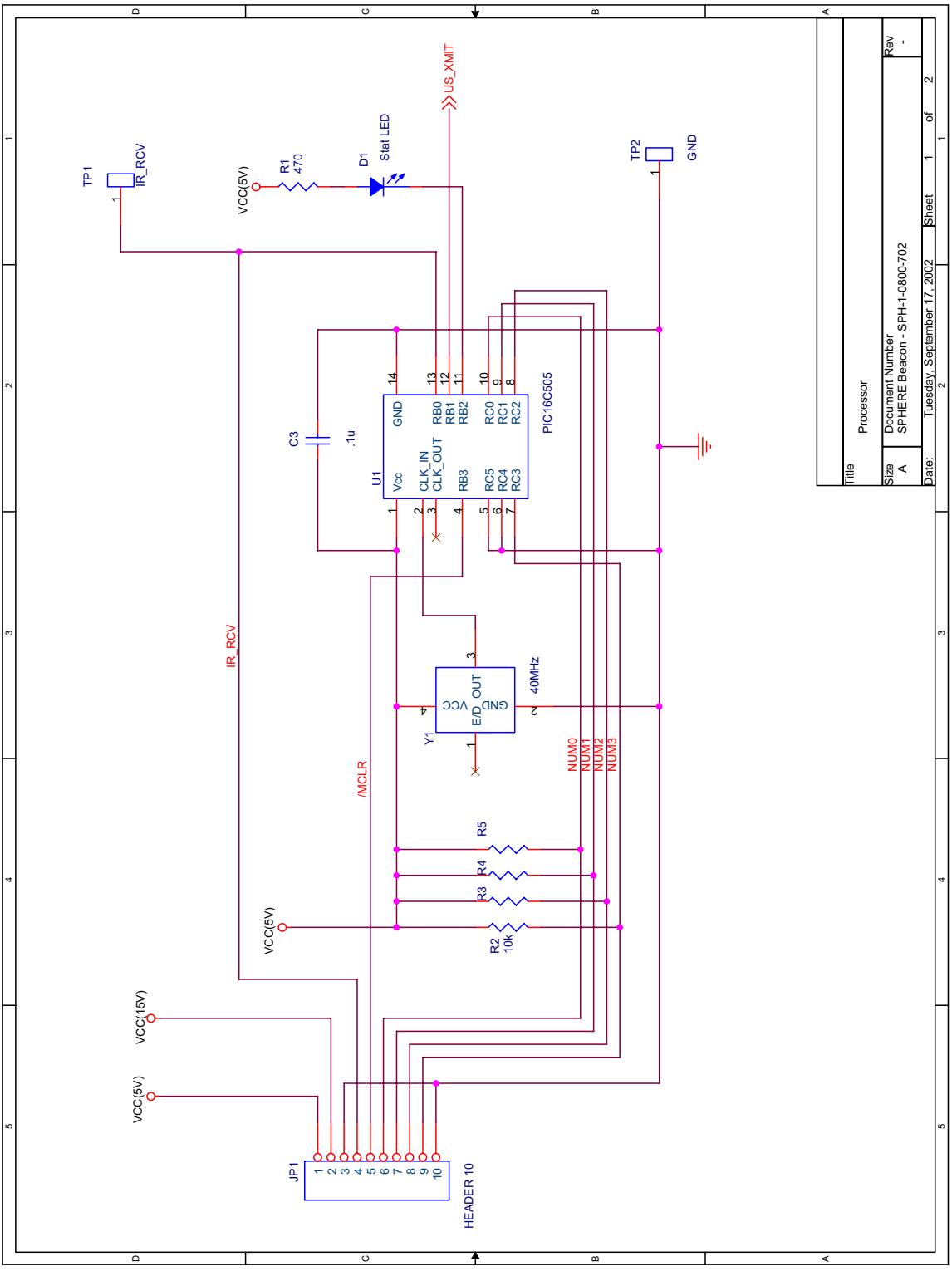
Date: Thursday, September 19, 2002
Sheet 9 of 9

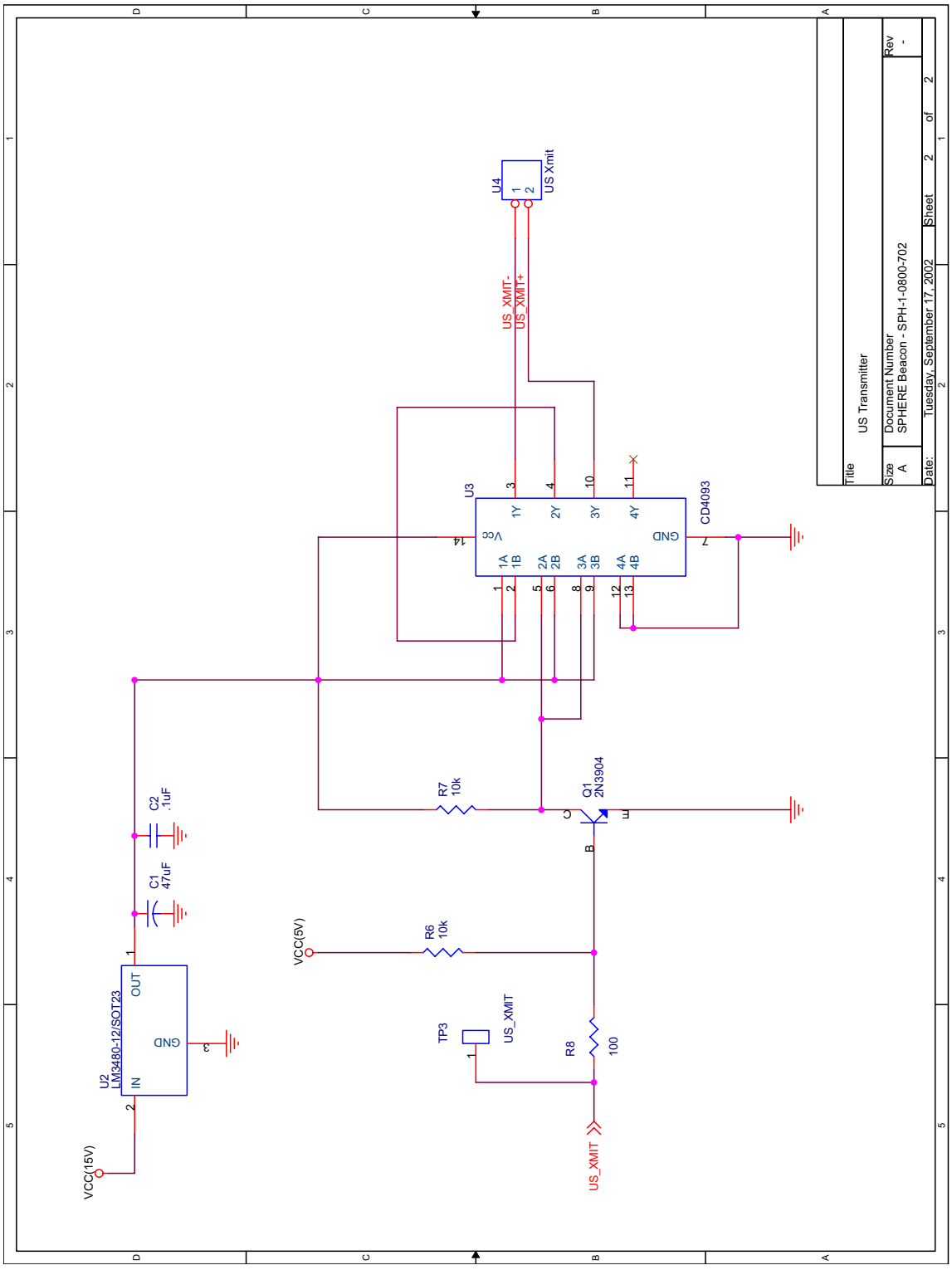

All the grounds in this diagram must be one single thick trace which connects the 470uF cap to the IRL520N
Title
Board Assembly
Size A
Document Number Metrology 6 - SPH-1-0800-101
Rev B
Date: Tuesday, February 18, 2003
Sheet 1 of 3
VCC(+5V)
R1 100 Ohm
C2 0.1uF
C3 47uF
D1 IR LED
D2 IR LED
R2 1 Ohm
R3 1 Ohm
D3
IRLML2502
R4 1M
IR XMIT
JP1 HEADER 10
C1 4.7uF bypass
VCC(+2.5V)
VCC(+5V)
R5 22K
R6 22K
C4 4.7uF bypass
US RCV 1
US RCV 2
US Signal
US Circuit
US-1
US-2
C14 4.7uF
C13 0.1uF
R27 47 Ohm
IR RCV
J1
IR PAD

Each metrology board includes two of these circuits:




J1
Accel
VCC(-15V)
VCC(15V)
VCC(5V)
R3
100k
R9
56.2k
R2
4.02M
C1
470p
U2
MAX409
R4
100k
R8
100k
R1
102k
R5
100k
R6
2k
R7
10.0k
U1
QA-750
Out
-V
+V
GND
Test
Temp
Title
Accelerometer Buffer/Amplifiers
Size
A
Document Number
Accel PCB - SPH-1-0800-205
Rev
B
Date:
Wednesday, September 18, 2002
Sheet
1
of
1


TP1
IR_RCV
VCC(5V)
R1
470
D1
Stat LED
US_XMIT
TP2
GND
C3
.1u
U1
PIC16C505
GND
Vcc
CLK_IN
CLK_OUT
RB0
RB1
RB2
RB3
RC0
RC1
RC2
RC3
RC4
RC5
Y1
GND
VCC
E/D
OUT
40MHz
IR_RCV
/MCLR
NUM0
NUM1
NUM2
NUM3
R5
R4
R3
R2
10k
VCC(5V)
VCC(15V)
VCC(5V)
JP1
HEADER 10
Title
Processor
Size
A
Document Number
SPHERE Beacon - SPH-1-0800-702
Rev
-
Date:
Tuesday, September 17, 2002
Sheet
1
of
2


U4
US Xmit
US_XMIT-
US_XMIT+
U3
CD4093
1Y
2Y
3Y
4Y
Vcc
GND
1A
1B
2A
2B
3A
3B
4A
4B
R7
10k
Q1
2N3904
C2
.1uF
C1
47uF
U2
LM3480-12/SOT23
OUT
GND
IN
VCC(15V)
VCC(5V)
R6
10k
TP3
US_XMIT
R8
100
US_XMIT
Title
US Transmitter
Size
A
Document Number
SPHERE Beacon - SPH-1-0800-702
Rev
-
Date:
Tuesday, September 17, 2002
Sheet
2
of
2

## F.1.5 Communications

### Design Drivers

- Two wireless communications channels
  - Satellite to Laptop (STL) - Telemetry and Commands
  - Satellite to Satellite (STS) - Control and Commands
- Support at least three satellites
- Should be expandable
- Accommodate a minimum volume of 6’ x 6’ x 6’
- Highest data rate possible
- Low power

### Functional Block Diagrams

Figure F.11 presents the functional block diagram of the communications sub-system. The major elements of the communications sub-system are three PIC processors that translate TI Commport signals into standard 8-bit (plus start and stop bit) UART serial data and two DR200x modules (one each for Satellite-to-Laptop {STL} and for Satellite-to-Satellite {STS} communications) which convert the 8-bit UART data into 14-bit bit-balanced words to minimize errors during wireless transmissions. The two elements are described below.

### DR200x Wireless Boards

The DR2000 development kit is a COTS product available from RFM Monolithics in. The kit utilizes an ARM DSP to manage data for wireless transmissions. The ARM performs four functions:

- Creates 12-bit bit-balanced words for every byte to be transmitted. Bit balanced words contain the same number of ones and zeros to reduce the error rate in wireless transmission.
- Manages packets of a pre-set size. The DR200x can be configured to send fixed sized packets immediately once the fixed number of bytes are received; alternatively, it will transmit a packet if there is a pause longer than 2ms between bytes.

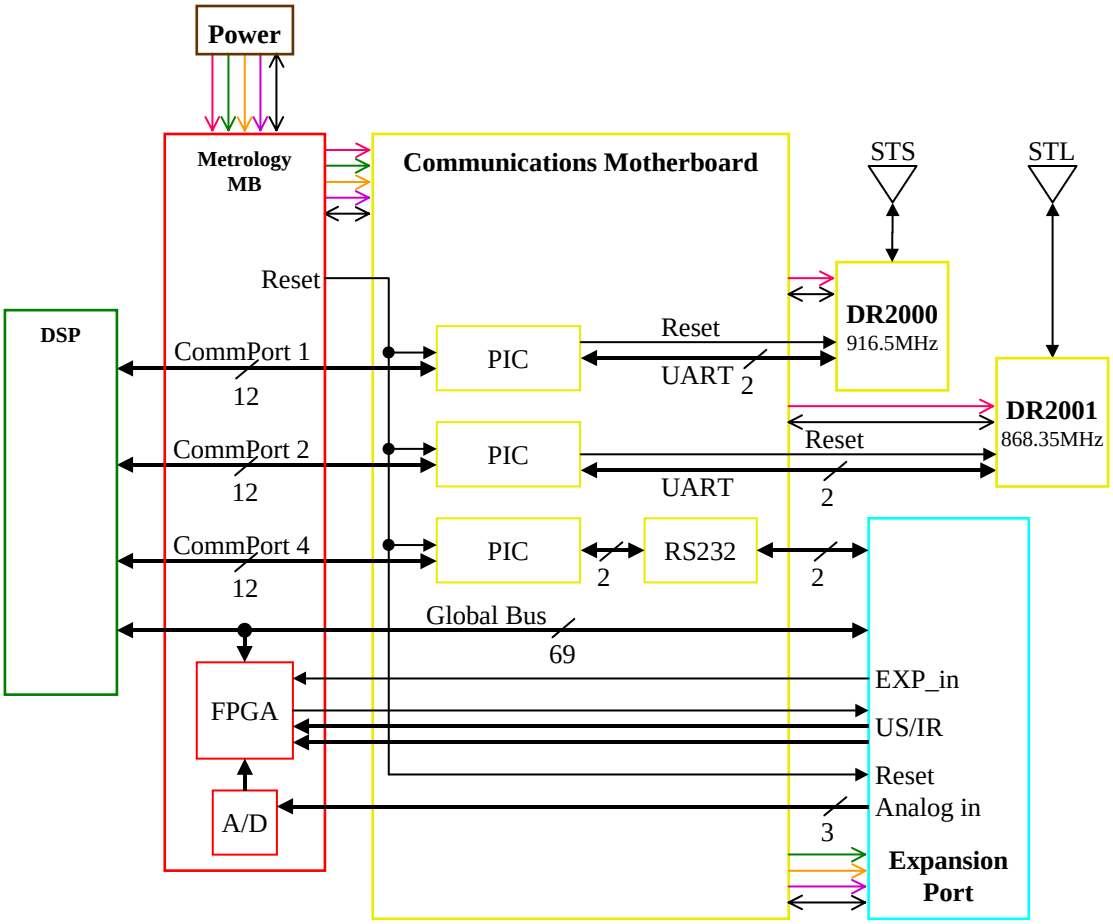



**Figure F.11** Communications sub-system functional block diagram

- Adds a start header to all transmissions which allows the crystals in the receiving end to resonate at the correct frequency before the actual data arrives.
- Allows identification of each module individually, so that data can be directed to a specific DR200x board.

The basic features of the DR200x boards are listed in Table F.10. Table F.11 describes the signals of the DR2000x.

To improve the bandwidth of the system, though, SPHERES uses custom firmware. Therefore, while [RFM, URL] provides an overview of the hardware used in the board, Appendix H should be consulted to understand the operations of firmware. Further, to

**TABLE F.10** DR200x specifications

| | DR2000 | DR2001 |
|---|---|---|
| Frequency | 916.5MHz | 868.35MHz |
| Maximum wireless data rate | 115.2kbps | |
| Implemented wireless data rate | 56.6kbps | |
| UART data rate | 115.2kbps | |
| Buffer | 64 bytes | |
| RF Mode | ASK | |
| Available Addresses | 1-255 (0x01-0xFF) | |
| Broadcast mode | Yes (to address = 0x00) | |
| Packet size | 1-255 (0x01-0xFF) | |
| Input Voltage | 3.1V-3.6V | |
| Power | <050mW | |

**TABLE F.11** DR200x signals descriptions

| Signal | Type | Description |
|---|---|---|
| Vcc(+3.3V) | Pwr | +3.3V power |
| GND | Pwr | Common ground |
| RX | Out | Serial data receive line |
| TX | In | Serial data transmit line |
| /RST | In | Reset |

minimize power consumption, the DR200x board used inside the satellites have been modified by removing the power regulation circuit (because the satellite power system provides regulated 3.3V) and the RS232 level converter, since the boards can connect directly through TTL to the PIC processors.

### Communications Interface Board

The communications interface board hosts the PIC processors which translate the DR200x serial data to the TI commport standard. The DR200x utilizes a standard UART signal at 115.2kbps; the selected PIC (16C66) contains a serial port capable of handling up to 1.25Mbps communications with support via special registers. The implemented firmware

provides 96-byte input and output buffers. The TI commport standard is a parallel bi-directional data bus with token handshaking. The data consists of 32-bit words split into four bytes. Four control lines are used to pass the token (REQ and ACK) between the two units (in this case the DSP and the PIC) and to indicate that data is available (STRB) and has been read (RDY). Chapter 8 of [TI, SPRU159A] describes the operations of the communications ports in full.

Table F.12 describes the input and output signals of the communications motherboard.

**TABLE F.12** Communications motherboard signals description

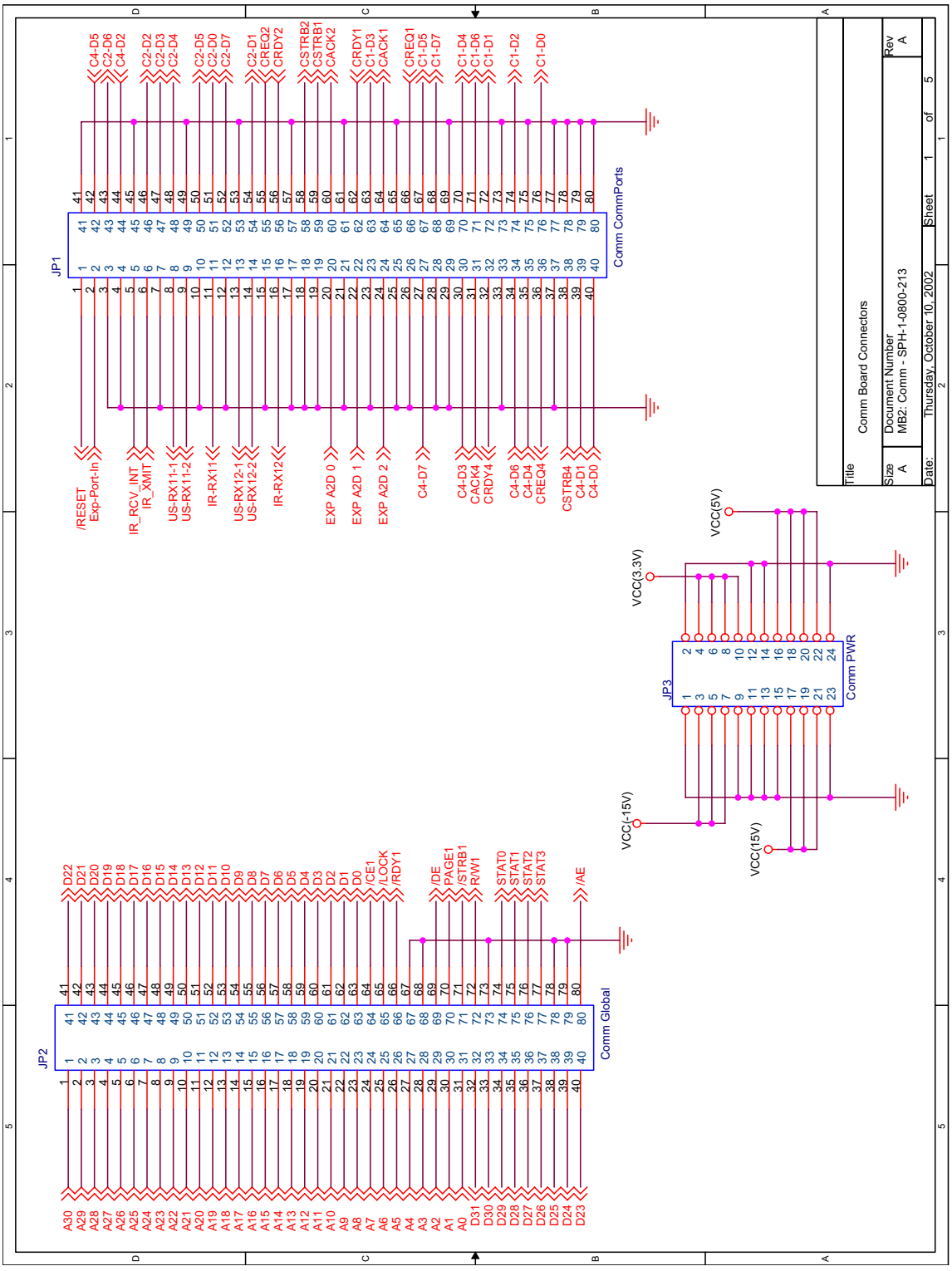
| Section | Signal | Type | Description |
|---|---|---|---|
| *To/From Metrology Mother-board* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+3.3V) | Pwr | +3.3V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |
| | A0-A30 | In | Global bus address lines (expansion port) |
| | D0-D31 | I/O | Global bus data lines (expansion port) |
| | RDY1 | I/O | Global bus ready (expansion port) |
| | PAGE1 | I/O | Global bus page select (expansion port) |
| | STRB1 | In | Global bus strobe (expansion port) |
| | R/W1 | I/O | Global bus read/write (expansion port) |
| | /RESET | In | Reset line |
| | /Exp_port_in | Out | Expansion port item indicator |
| | IR_XMIT | In | IR transmit command |
| | US-RX[11-12]-[1-2] | Out | Input ultrasound signals from the expansion port board |
| | IR-RX[11-12] | Out | Input infrared signals from the expansion port board |
| | EXP A2D [0-2] | Out | Analog signals from expansion port |
| | C[1,2,4] D[0-7] | I/O | Commport data lines |
| | CACK[1,2,4] | I/O | Commport acknowledge signal |
| | CRDY[1,2,4] | I/O | Commport ready signal |

**TABLE F.12** Communications motherboard signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Met. MB (cont)* | CREQ[1,2,4] | I/O | Commport request signal |
| | STRB[1,2,4] | I/O | Commport strobe |
| *Expansion Port Connector* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |
| | A0-A30 | Out | Global bus address lines |
| | D0-D31 | I/O | Global bus data lines |
| | RDY1 | I/O | Global bus ready |
| | PAGE1 | I/O | Global bus page select |
| | STRB1 | Out | Global bus strobe |
| | R/W1 | I/O | Global bus read/write |
| | /RESET | In | Reset line |
| | /Exp_port_in | In | High when an expansion port selects to bypass the satellite US/IR metrology boards |
| | IR_XMIT | Out | IR transmit command |
| | US-RX[11-12]-[1-2] | In | Input ultrasound signals |
| | IR-RX[11-12] | In | Input infrared signals |
| | EXP A2D [0-2] | In | Input analog signals |
| | EXP RX | In | Serial data receive (RS232) |
| | EXP TX | Out | Serial data transmit (RS232) |
| *Wired Serial Connector* | EXP RX | In | Serial data receive (RS232) |
| | EXP TX | Out | Serial data transmit (RS232) |
| | GND | Pwr | Common Ground |
| *DR200x (2x)* | Vcc(+3.3V) | Pwr | +3.3V power |
| | GND | Pwr | Common ground |
| | RX | Out | Serial data receive line |
| | TX | In | Serial data transmit line |
| | /RST | In | Reset |

## Schematics

The schematics of the DR200x boards are available in [RFM, URL]. The schematics of the SPHERES communications motherboard are presented next.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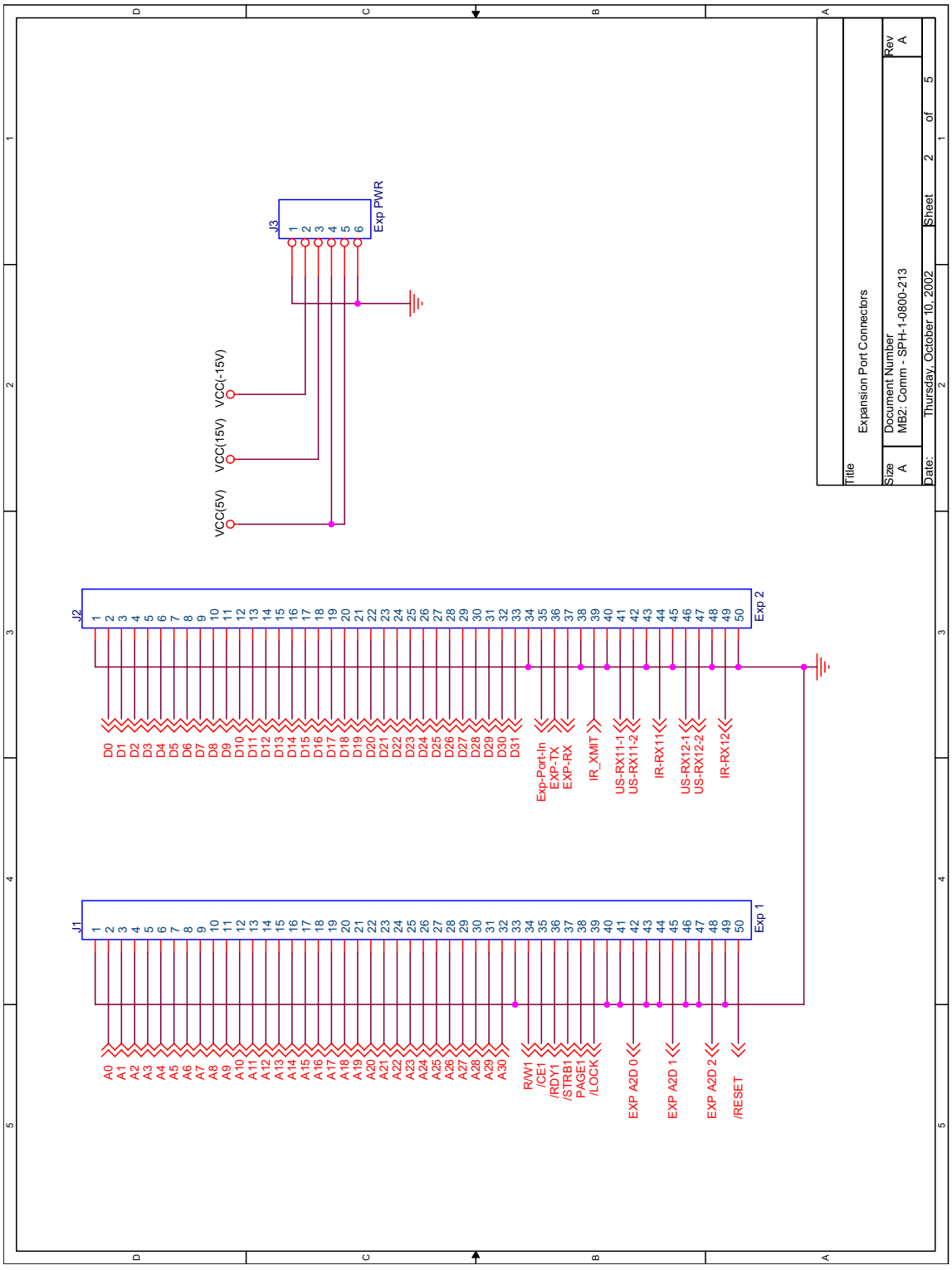
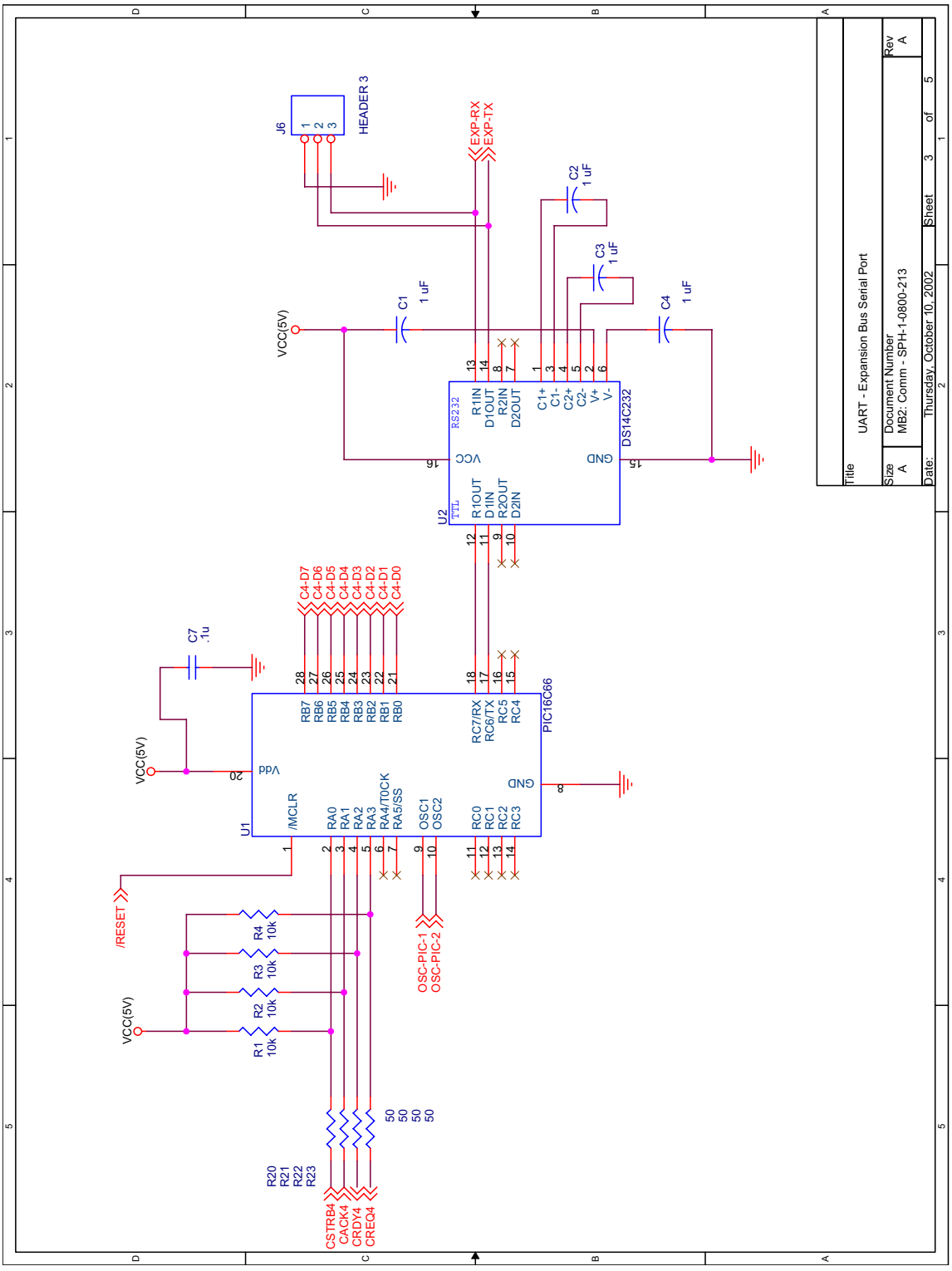
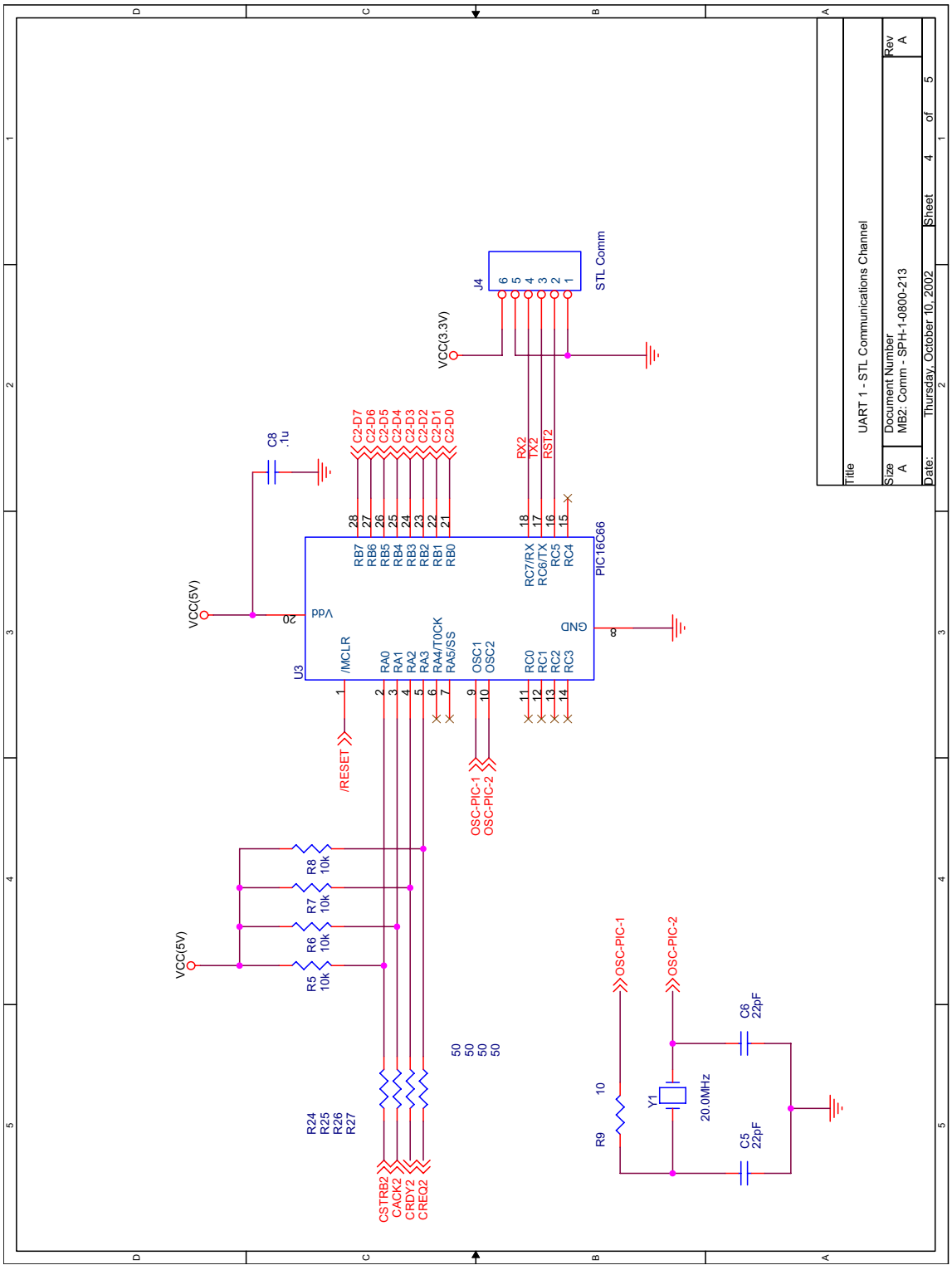
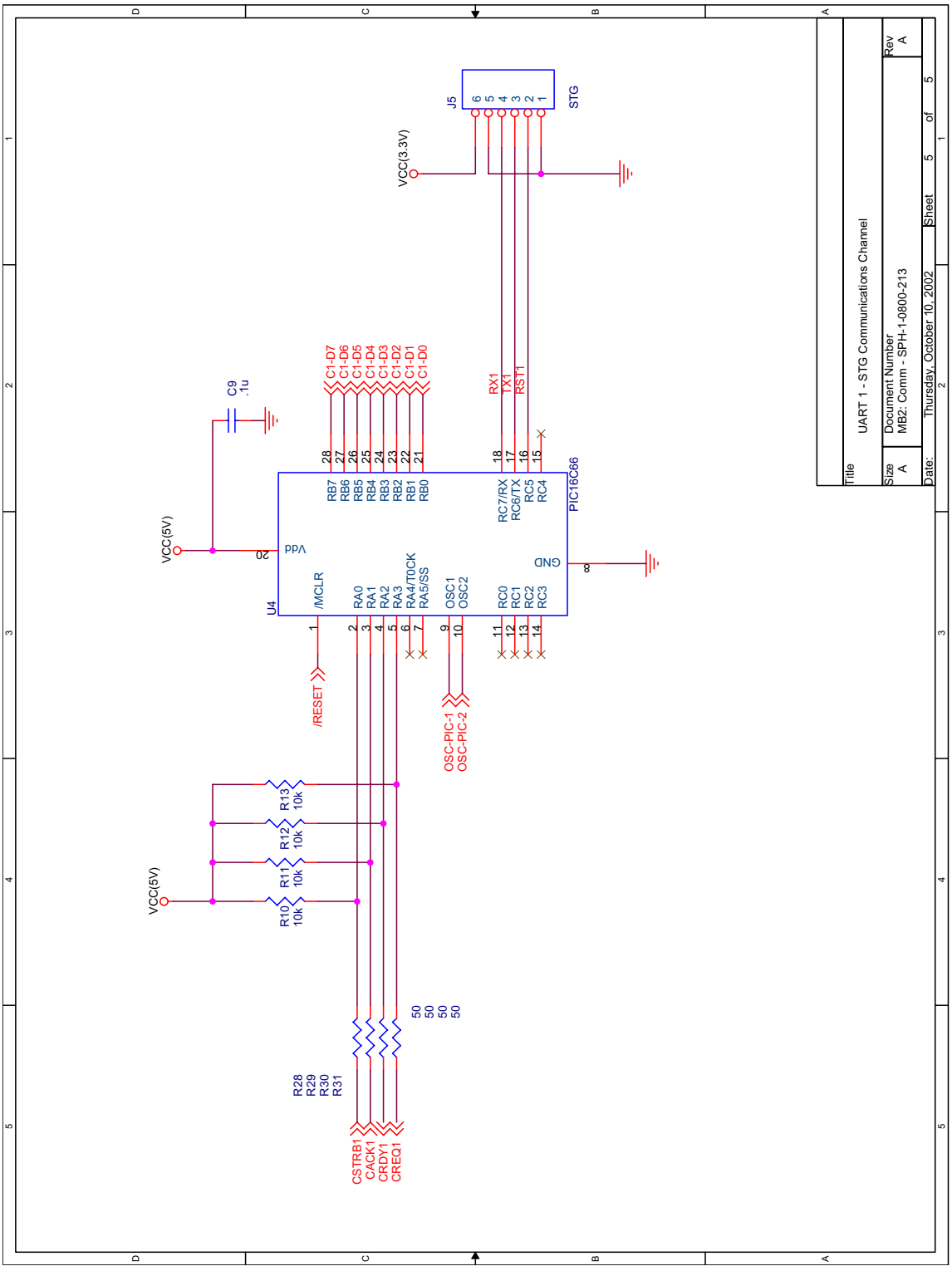
Comm CommPorts
/RESET
Exp-Port-Int
IR_RCV_INT
IR_XMIT
US-RX11-1
US-RX11-2
IR-RX11
US-RX12-1
US-RX12-2
IR-RX12
EXP A2D 0
EXP A2D 1
EXP A2D 2
C4-D7
C4-D3
CACK4
CRDY4
C4-D6
C4-D4
CREQ4
CSTRB4
C4-D1
C4-D0
C4-D5
C2-D6
C4-D2
C2-D2
C2-D3
C2-D4
C2-D5
C2-D0
C2-D7
C2-D1
CREQ2
CRDY2
CSTRB2
CSTRB1
CACK2
CRDY1
C1-D3
CACK1
CREQ1
C1-D5
C1-D7
C1-D4
C1-D6
C1-D1
C1-D2
C1-D0
JP2
Comm Global
A30
A29
A28
A27
A26
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
/CE1
/LOCK
/RDY1
/DE
PAGE1
/STRB1
R/W1
STAT0
STAT1
STAT2
STAT3
/AE
JP3
Comm PWR
VCC(3.3V)
VCC(5V)
VCC(-15V)
VCC(15V)
Title
Comm Board Connectors
Size
A
Document Number
MB2: Comm - SPH-1-0800-213
Rev
A
Date:
Thursday, October 10, 2002
Sheet
1
of
5


Title
Expansion Port Connectors
Size
A
Document Number
MB2: Comm - SPH-1-0800-213
Rev
A
Date:
Thursday, October 10, 2002
Sheet
2
of
5
J3
Exp PWR
VCC(-15V)
VCC(15V)
VCC(5V)
J2
Exp 2
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
Exp-Port-In
EXP-TX
EXP-RX
IR_XMIT
US-RX11-1
US-RX11-2
IR-RX11
US-RX12-1
US-RX12-2
IR-RX12
J1
Exp 1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
A30
R/W1
/CE1
/RDY1
/STRB1
PAGE1
/LOCK
EXP A2D 0
EXP A2D 1
EXP A2D 2
/RESET


HEADER 3
J6
EXP-RX
EXP-TX
C2
1 uF
C3
1 uF
C4
1 uF
C1
1 uF
VCC(5V)
U2
DS14C232
R1IN
D1OUT
R2IN
D2OUT
C1+
C1-
C2+
C2-
V+
V-
VCC
GND
R1OUT
D1IN
R2OUT
D2IN
C4-D7
C4-D6
C4-D5
C4-D4
C4-D3
C4-D2
C4-D1
C4-D0
C7
.1u
U1
PIC16C66
/MCLR
Vdd
GND
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
RC7/RX
RC6/TX
RC5
RC4
RA0
RA1
RA2
RA3
RA4/T0CK
RA5/SS
OSC1
OSC2
RC0
RC1
RC2
RC3
/RESET
R4
10k
R3
10k
R2
10k
R1
10k
OSC-PIC-1
OSC-PIC-2
R20
R21
R22
R23
50
50
50
50
CSTRB4
CACK4
CRDY4
CREQ4
Title
UART - Expansion Bus Serial Port
Size
A
Document Number
MB2: Comm - SPH-1-0800-213
Rev
A
Date:
Thursday, October 10, 2002
Sheet
3
of
5


Title
UART 1 - STL Communications Channel
Size
A
Document Number
MB2: Comm - SPH-1-0800-213
Rev
A
Date:
Thursday, October 10, 2002
Sheet
4
of
5
STL Comm
J4
VCC(3.3V)
PIC16C66
U3
VCC(5V)
C8
.1u
/MCLR
/RESET
OSC-PIC-1
OSC-PIC-2
R5
R6
R7
R8
10k
R24
R25
R26
R27
50
CSTRB2
CACK2
CRDY2
CREQ2
R9
10
Y1
20.0MHz
C5
22pF
C6
22pF


Title
UART 1 - STG Communications Channel
Size
A
Document Number
MB2: Comm - SPH-1-0800-213
Rev
A
Date:
Thursday, October 10, 2002
Sheet
5
of
5
J5
STG
VCC(3.3V)
C9
.1u
VCC(5V)
U4
PIC16C66
/MCLR
VDD
VSS
GND
RA0
RA1
RA2
RA3
RA4/T0CK
RA5/SS
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
RC7/RX
RC6/TX
RC5
RC4
RC0
RC1
RC2
RC3
OSC1
OSC2
C1-D7
C1-D6
C1-D5
C1-D4
C1-D3
C1-D2
C1-D1
C1-D0
RX1
TX1
RST1
/RESET
OSC-PIC-1
OSC-PIC-2
R10 10k
R11 10k
R12 10k
R13 10k
R28 50
R29 50
R30 50
R31 50
CSTRB1
CACK1
CRDY1
CREQ1

## F.1.6 Expansion Port

### Design Drivers

- Provide digital interface for future expansions

### Functional Block Diagrams

The broad requirements in the definition of the expansion port resulted in a design which provides a simple but limited serial line capable of up to 1.25Mbps data rates as well as the very flexible but complex global bus. Figure F.12 presents the functional block diagram for the Expansion Port.

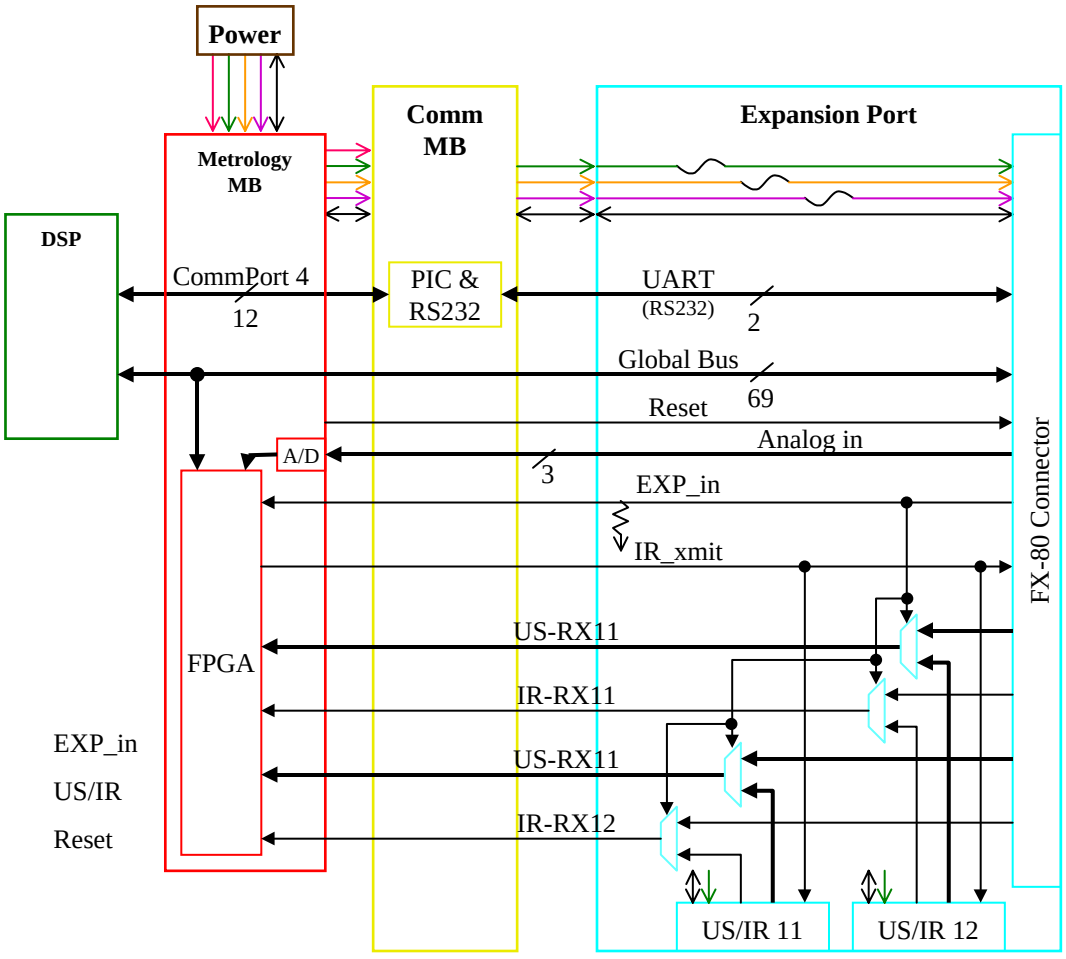



**Figure F.12** Expansion port functional block diagram

Apart from providing the required digital data lines, the Expansion Port also supports three other functions:

- Provides power to expansion items via +5V, +15V, and -15V power lines. It protects these lines with 0.5A self-resetable fuses.
- Because three analog lines were available from the basic metrology design, the expansion port makes these lines available to expansion items.
- Allows an expansion item to *bypass* the internal US/IR metrology boards located on the expansion port face (+X face). This allows an expansion item to replace the functionality of those boards if the expansion item covers the sensors. The expansion board uses high-speed multiplexers so that the signals received by the FPGA are equivalent to any other US/IR signals. The EXP_in line allows the DSP to account for the new physical locations (which must be programmed) of the US/IR boards when the signals have been bypassed.

Table F.13 describes the inputs and outputs of the Expansion Port.

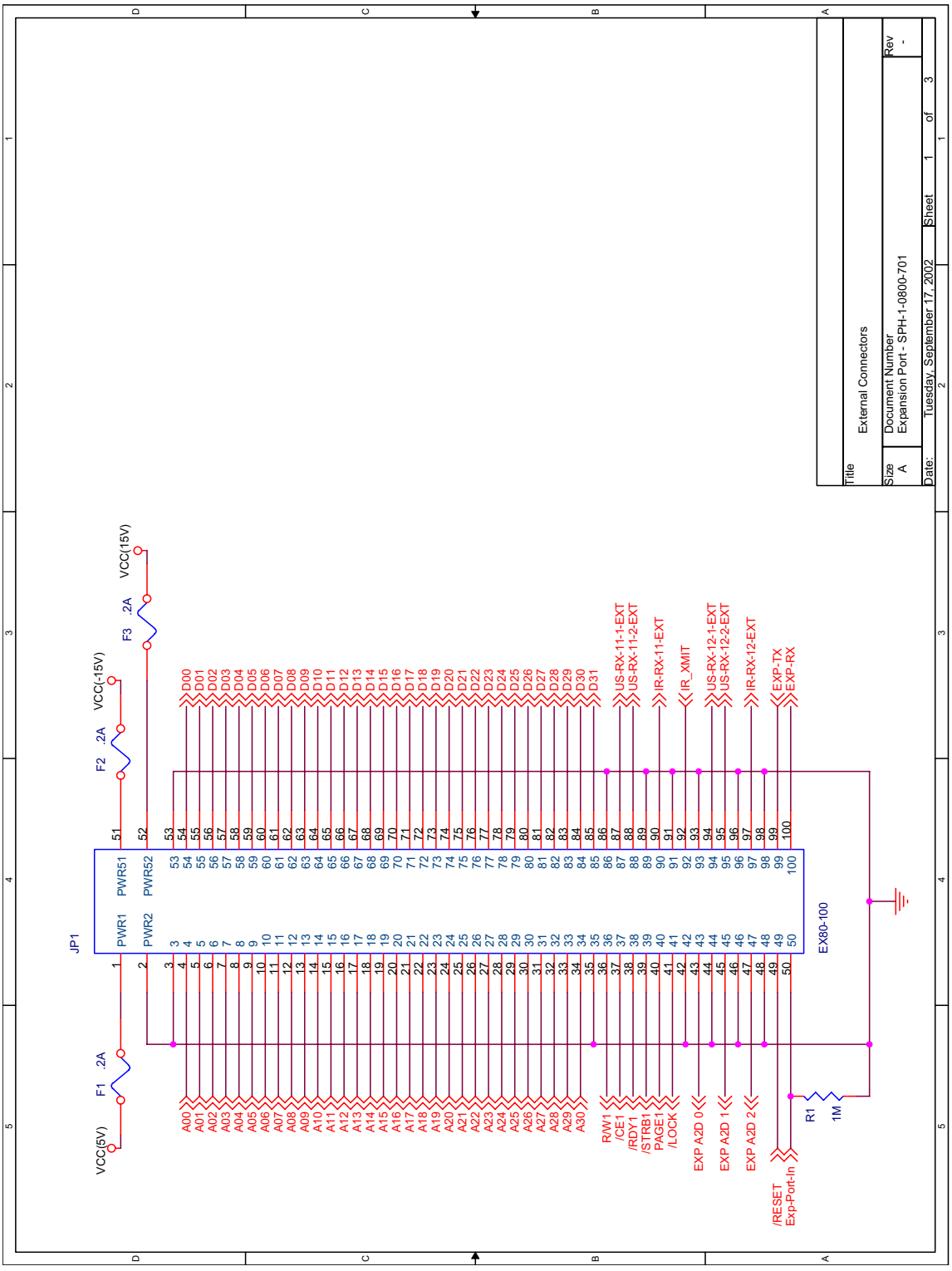
**TABLE F.13** Expansion port signals description

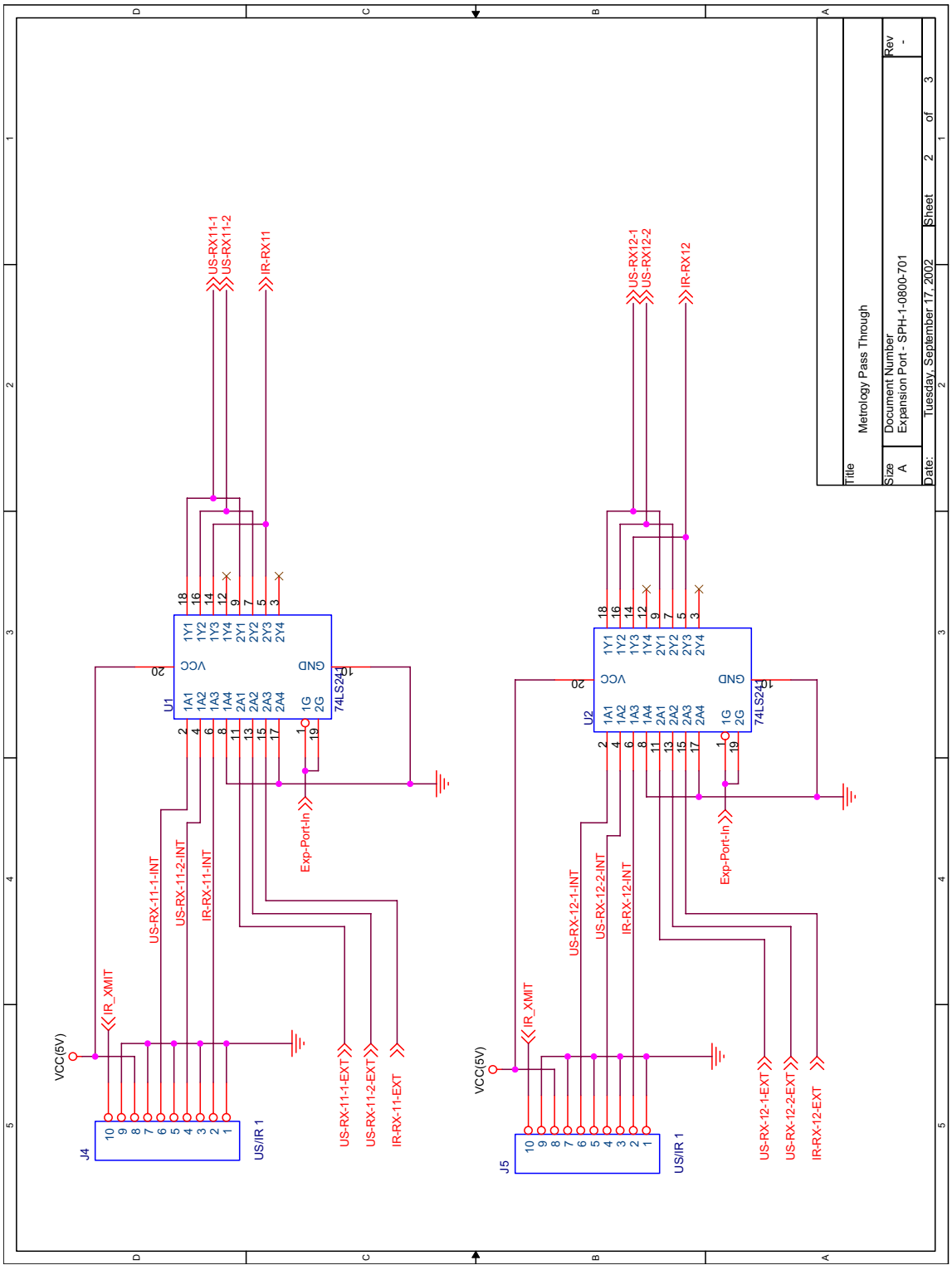
| Section | Signal | Type | Description |
|---|---|---|---|
| *To/From Comm. Mother-board* | *See Table F.12* | | |
| *Expansion Port Con-nector* | Vcc(+5V) | Pwr | +5V power |
| | Vcc(+15V) | Pwr | +15V power |
| | Vcc(-15V) | Pwr | -15V power |
| | GND | Pwr | Common ground |
| | A0-A30 | Out | Global bus address lines |
| | D0-D31 | I/O | Global bus data lines |
| | RDY1 | I/O | Global bus ready |
| | PAGE1 | I/O | Global bus page select |
| | STRB1 | Out | Global bus strobe |
| | R/W1 | I/O | Global bus read/write |
| | /RESET | In | Reset line |

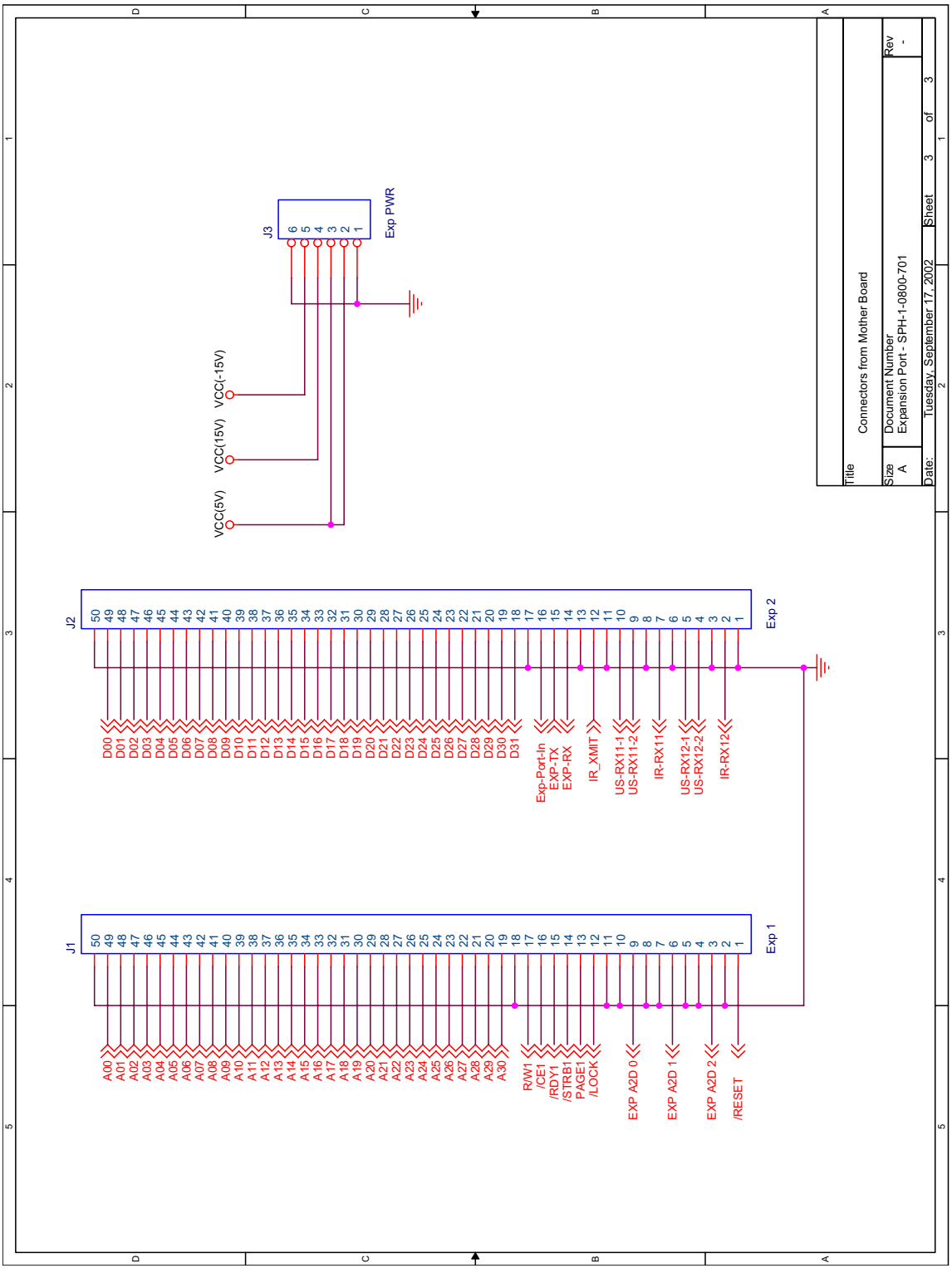
**TABLE F.13** Expansion port signals description

| Section | Signal | Type | Description |
|---|---|---|---|
| *Expansion Port (cont)* | /Exp_port_in | In | High when an expansion port selects to bypass the satellite US/IR metrology boards |
| | IR_XMIT | Out | IR transmit command |
| | US-RX[11-12]-[1-2]-EXT | In | External sensor input ultrasound signals |
| | IR-RX[11-12]-EXT | In | External sensor input infrared signals |
| | EXP A2D [0-2] | In | Input analog signals |
| | EXP RX | In | Serial data receive (RS232) |
| | EXP TX | Out | Serial data transmit (RS232) |
| *Metrology Pass-through (2x)* | Vcc(+5V) | Pwr | +5V power |
| | GND | Pwr | Common ground |
| | IR_XMIT | Out | IR transmit command |
| | US-RX[11-12]-[1-2]-INT | In | Internal sensor input ultrasound signals |
| | IR-RX[11-12]-INT | In | Internal sensor input infrared signals |

## Schematics


JP1
EX80-100
PWR1
PWR2
PWR51
PWR52
F1 .2A
F2 .2A
F3 .2A
VCC(5V)
VCC(-15V)
VCC(15V)
R1
1M
R/W1
/CE1
/RDY1
/STRB1
PAGE1
/LOCK
EXP A2D 0
EXP A2D 1
EXP A2D 2
/RESET
Exp-Port-In
IR_XMIT
IR-RX-11-EXT
IR-RX-12-EXT
US-RX-11-1-EXT
US-RX-11-2-EXT
US-RX-12-1-EXT
US-RX-12-2-EXT
EXP-TX
EXP-RX
Title
External Connectors
Size
A
Document Number
Expansion Port - SPH-1-0800-701
Rev
-
Date:
Tuesday, September 17, 2002
Sheet
1
of
3


Title
Metrology Pass Through
Size
A
Document Number
Expansion Port - SPH-1-0800-701
Rev
-
Date:
Tuesday, September 17, 2002
Sheet
2
of
3
US-RX11-1
US-RX11-2
IR-RX11
U1
74LS241
VCC
GND
1G
2G
Exp-Port-In
US-RX-11-1-INT
US-RX-11-2-INT
IR-RX-11-INT
IR_XMIT
VCC(5V)
J4
US/IR 1
US-RX-11-1-EXT
US-RX-11-2-EXT
IR-RX-11-EXT
US-RX12-1
US-RX12-2
IR-RX12
U2
US-RX-12-1-INT
US-RX-12-2-INT
IR-RX-12-INT
J5
US-RX-12-1-EXT
US-RX-12-2-EXT
IR-RX-12-EXT


Connectors from Mother Board
Expansion Port - SPH-1-0800-701
Tuesday, September 17, 2002
Exp PWR
VCC(5V)
VCC(15V)
VCC(-15V)
Exp 1
Exp 2
A00 A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31
R/W1
/CE1
/RDY1
/STRB1
PAGE1
/LOCK
EXP A2D 0
EXP A2D 1
EXP A2D 2
/RESET
Exp-Port-In
EXP-TX
EXP-RX
IR_XMIT
US-RX11-1
US-RX11-2
IR-RX11
US-RX12-1
US-RX12-2
IR-RX12

## F.2 Laptop Communications

### Design Drivers

- Interface with standard equipment available on the ISS SSC

### Functional Block Diagrams

The laptop transceiver is a modified DR2001 (868.35MHz) development kit (the backup is a DR2000, 916.5MHz). The transceiver uses the custom firmware developed for SPHERES and does not use the power regulation circuit. The power regulation has been replaced with two diodes which step down the +5V voltage of a USB port of the SSC to approximately 3.6V, the maximum allowed by the DR200x without power circuitry.Figure F.13 presents the functional block diagram of the laptop communications. [RFM, URL] provides information on the hardware design, and Appendix H on the firmware and operations.

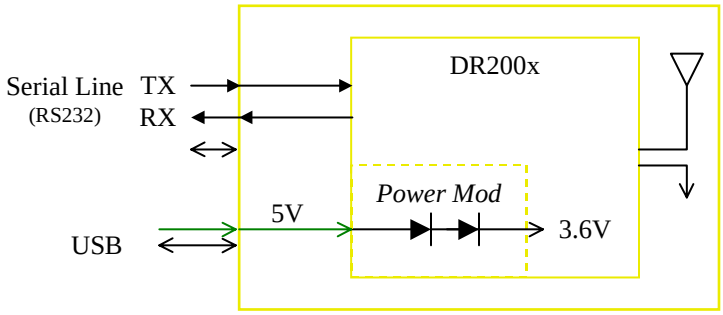



**Figure F.13** Laptop communications functional block diagram

## F.3 Metrology Beacons

### Design Drivers

- Trigger on IR reception
- Transmit ultrasonic (US) pulse at
  - $\Delta t = \{(N-1)\cdot 20 + 5\}$ ms
  - $N$ = beacon number (1-5)
- Provide selectable beacon number

- Battery operation
  - On/off switch
  - Low battery LED

**Functional Block Diagrams**

The metrology beacons operate on two AA batteries (alkaline aboard the ISS, which provide approximately 24 hours of operation, and rechargeable in ground-based facilities). The approximately 3V from the batteries are stepped-up to 5V to power a PIC microcontroller and 12V to drive the ultrasound transmitter. The PIC operates at 40MHz to create the pulses required for the ultrasound with a timing accuracy (as per the function presented in the design drivers) of 1μs (0.3mm error). The PIC creates a pulse with 16 oscillations at 40kHz. The driver circuitry effectively produces 24V pulses at the ultrasound transmitter by alternating the two leads of the transmitter between ground and +12V during the pulses (rather than using a 12V signal by holding one lead constant and only alternating the other lead). When there are no pulses a constant 12V differential exists between the leads, but the transmitter does not produce any ultrasound since it is a resonator which must be exited to its resonant frequency (40kHz). The beacon uses the same IR receiver/amplifier used in the satellite US/IR boards.

Two LED’s provide feedback on the status of the beacon. A green LED indicates the status of the beacon. A solid green indicated the beacon is powered on; a flashing green indicates the beacon is active (is transmitting ultrasound). An amber LED indicates a low-batter condition.

The functional block diagram of the metrology beacons is presented in Figure F.14.

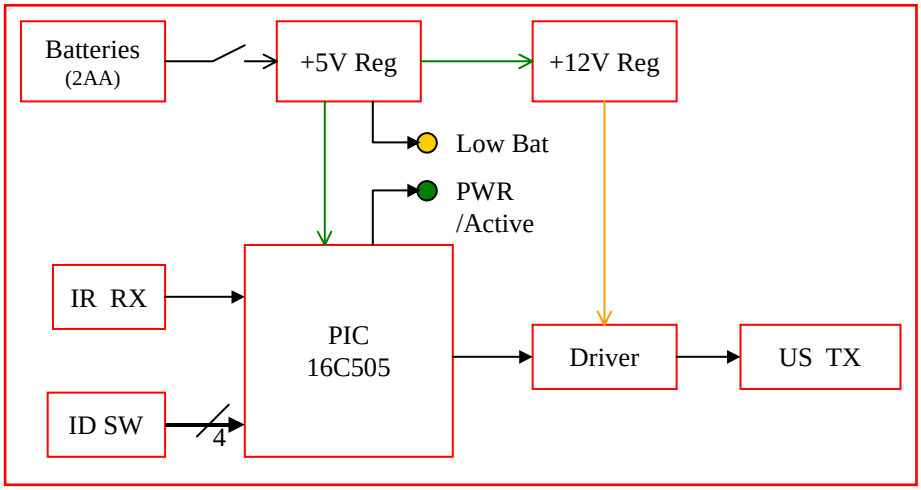
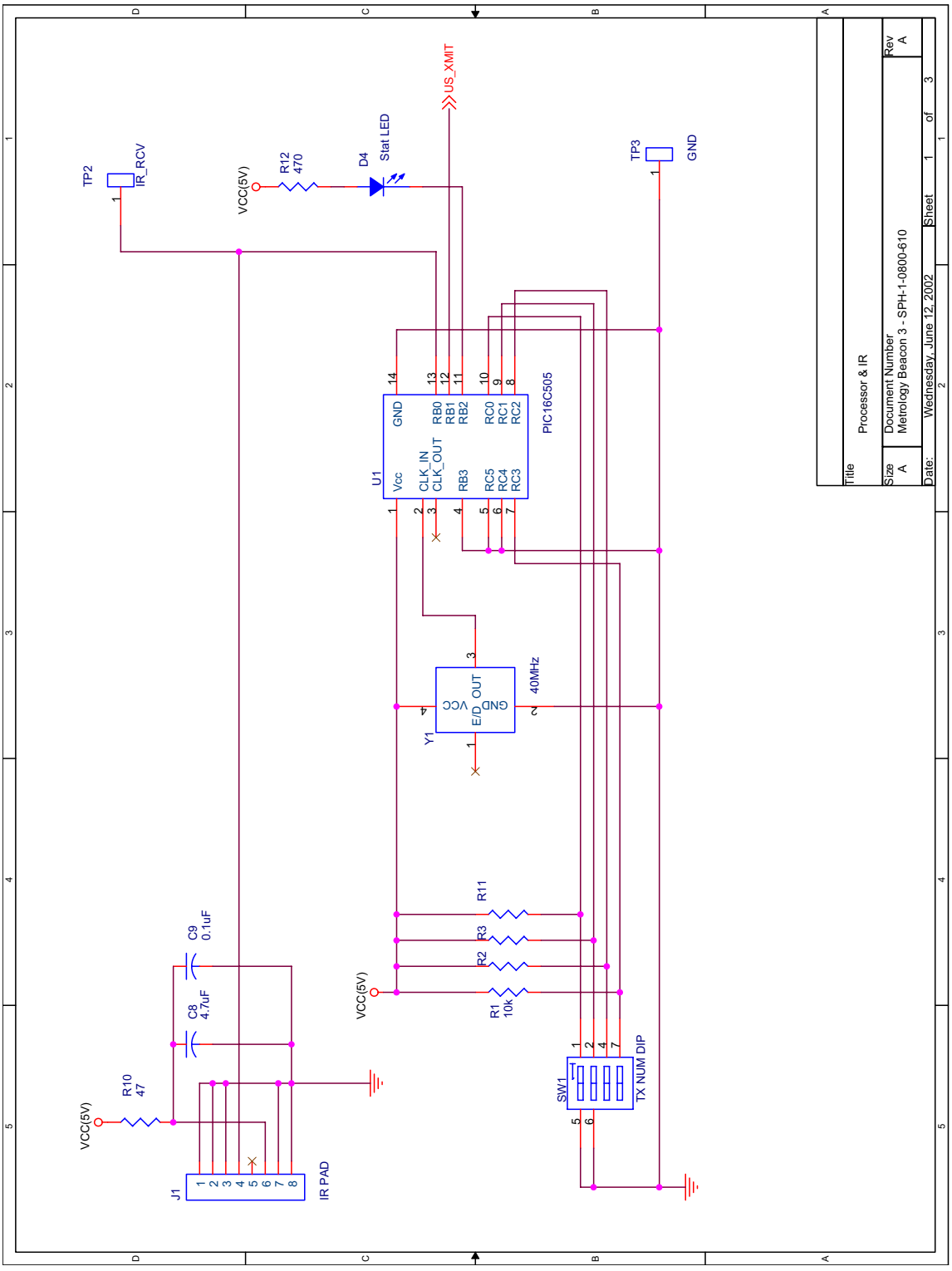



**Figure F.14** Metrology beacon functional block diagram

## Schematics


US_XMIT
TP2
IR_RCV
VCC(5V)
R12
470
D4
Stat LED
TP3
GND
U1
PIC16C505
GND
Vcc
CLK_IN
CLK_OUT
RB0
RB1
RB2
RB3
RC0
RC1
RC2
RC3
RC4
RC5
Y1
40MHz
E/D
OUT
R11
R3
R2
R1
10k
SW1
TX NUM DIP
C9
0.1uF
C8
4.7uF
R10
47
J1
IR PAD
Title
Processor & IR
Size
A
Document Number
Metrology Beacon 3 - SPH-1-0800-610
Rev
A
Date:
Wednesday, June 12, 2002
Sheet
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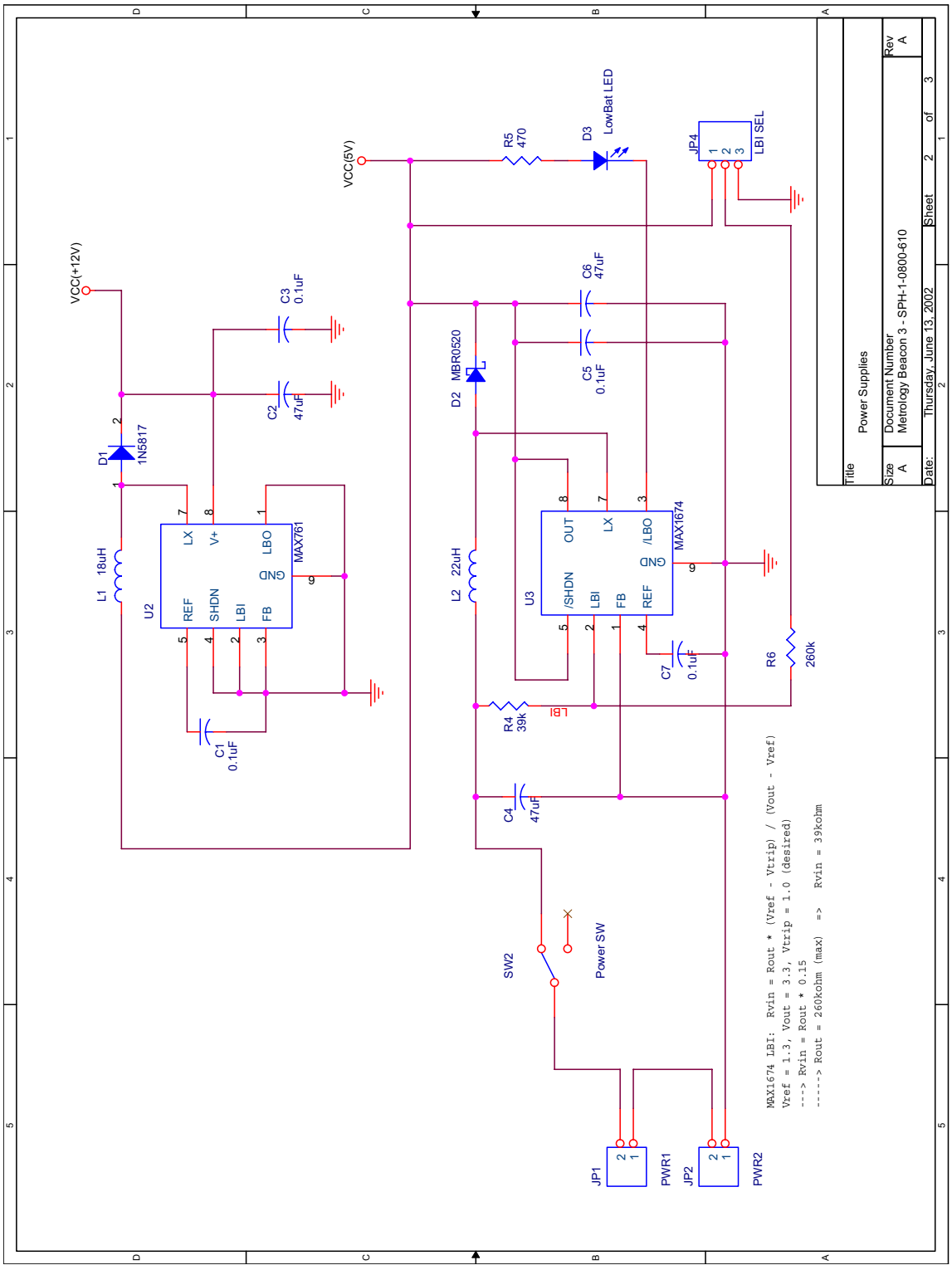
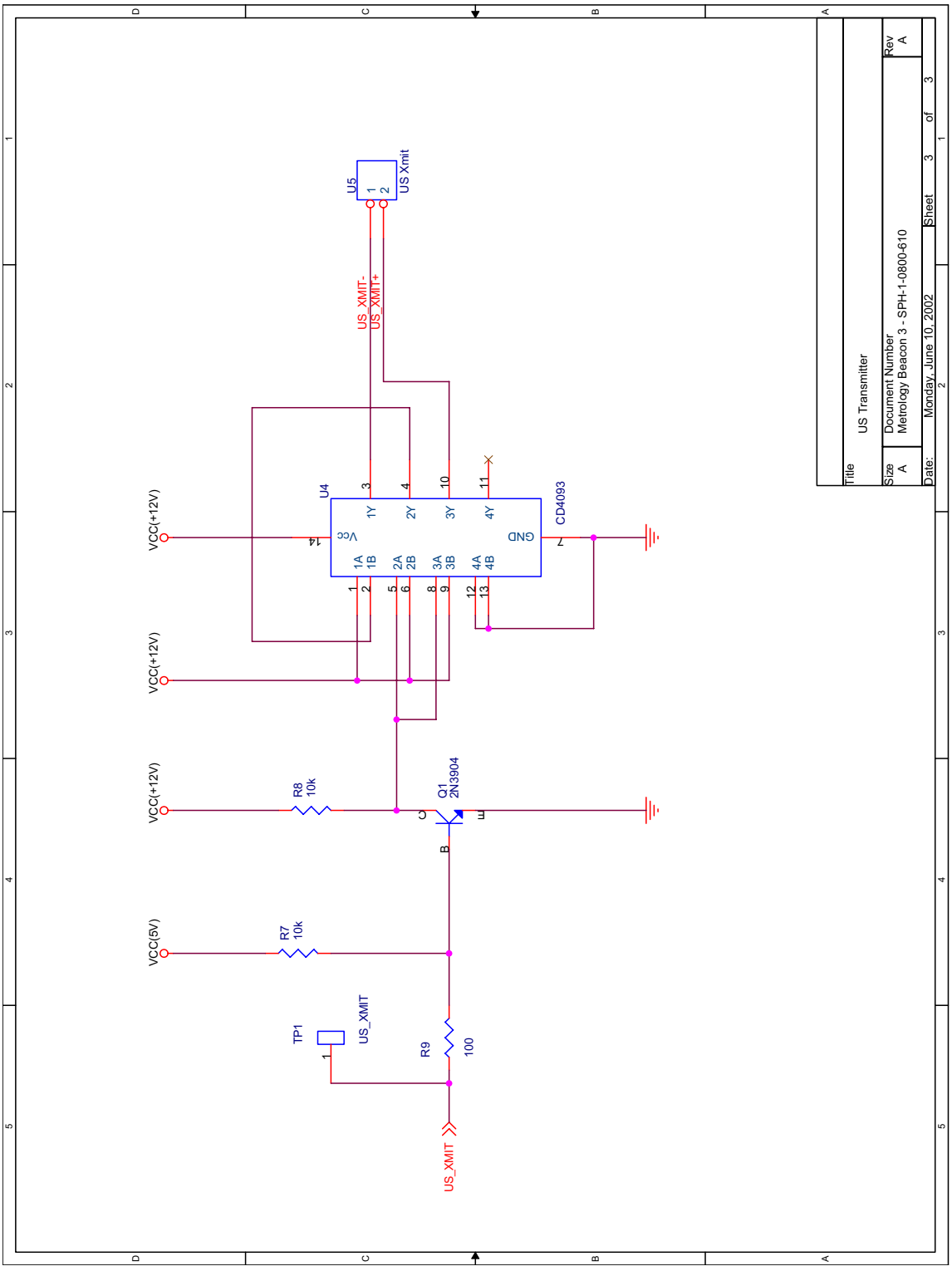
3


VCC(+12V)
VCC(5V)
D1 1N5817
D2 MBR0520
D3 LowBat LED
R5 470
JP4 LBI SEL
C3 0.1uF
C2 47uF
C6 47uF
C5 0.1uF
L1 18uH
L2 22uH
U2 MAX761
U3 MAX1674
REF SHDN LBI FB LX V+ LBO GND
OUT /SHDN LBI FB REF LX /LBO GND
C1 0.1uF
C7 0.1uF
C4 47uF
R4 39k
R6 260k
LBI
SW2
Power SW
JP1
JP2
PWR1
PWR2
MAX1674 LBI: Rvin = Rout * (Vref - Vtrip) / (Vout - Vref)
Vref = 1.3, Vout = 3.3, Vtrip = 1.0 (desired)
---> Rvin = Rout * 0.15
-----> Rout = 260kohm (max) => Rvin = 39kohm
Title Power Supplies
Size A
Document Number Metrology Beacon 3 - SPH-1-0800-610
Rev A
Date: Thursday, June 13, 2002
Sheet 2 of 3


U5
US Xmit
US_XMIT-
US_XMIT+
U4
CD4093
VCC(+12V)
VCC(+12V)
VCC(+12V)
VCC(5V)
R8
10k
R7
10k
Q1
2N3904
TP1
US_XMIT
R9
100
US_XMIT
Title
US Transmitter
Size
A
Document Number
Metrology Beacon 3 - SPH-1-0800-610
Rev
A
Date:
Monday, June 10, 2002
Sheet
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of
3

## F.4 Metrology Beacon Tester

### Design Drivers

- Allow operator to test each metrology beacon individually
  - Manual operation
  - Indicate beacon number
- Detect extraneous infrared and ultrasound signal in operational environment

### Functional Block Diagrams

The beacon tester merges the design of the satellites US/IR boards and the metrology beacons to allow an operator to determine correct operations of the metrology beacons. The design uses the same infrared receiver product as the satellites and beacons. It uses the same ultrasound amplification and infrared transmission electronics as the satellites. The beacon tester uses the same PIC processor used in the beacons to create an infrared signal, detect the ultrasound signals, and measure the time of flight to identify the beacon number. Figure F.15 presents the functional block diagram of the beacon tester.

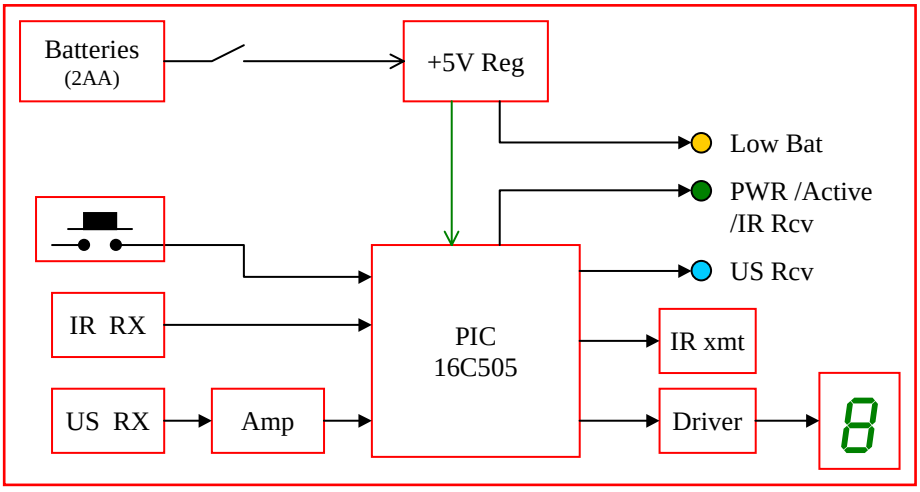
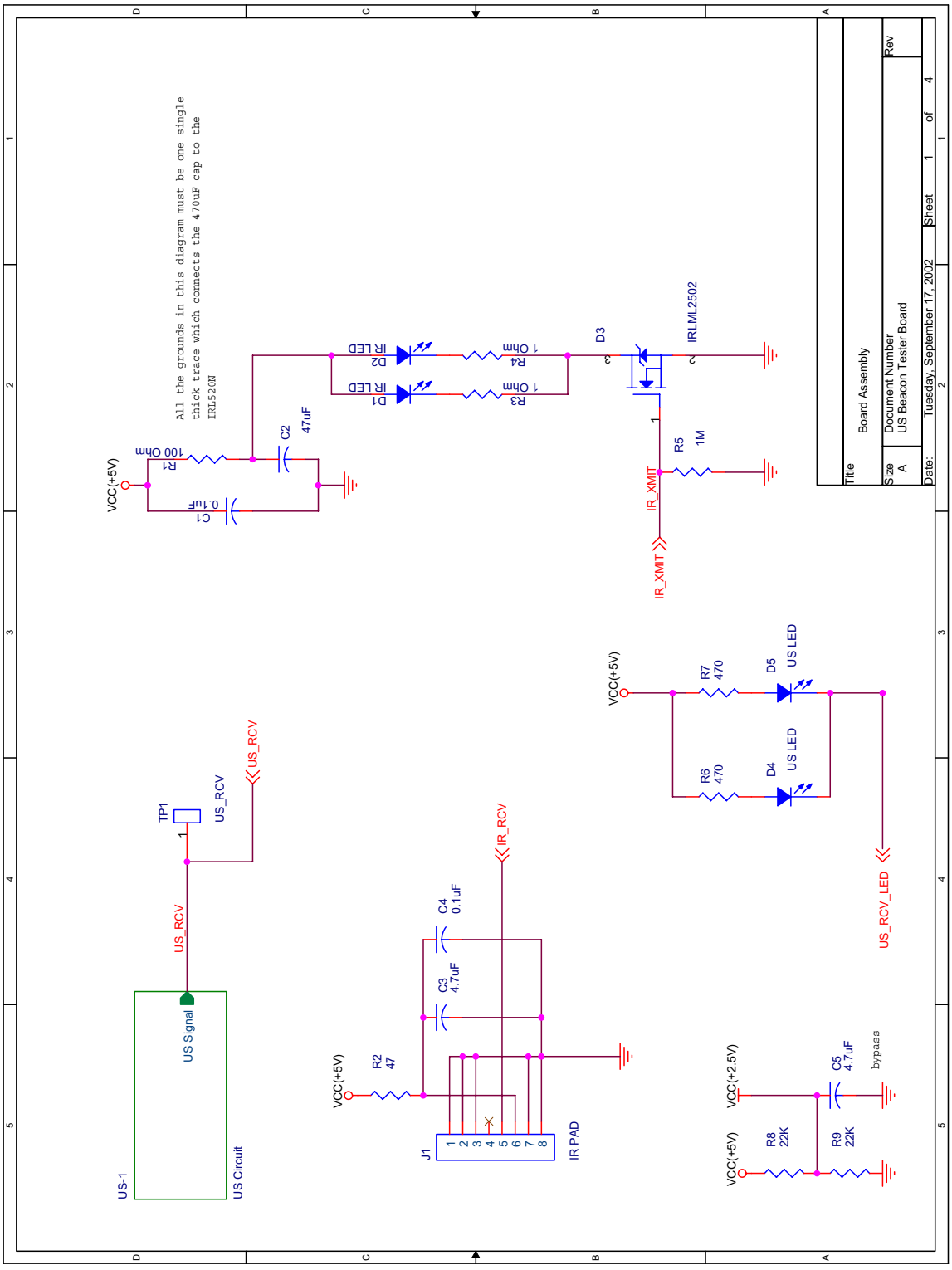


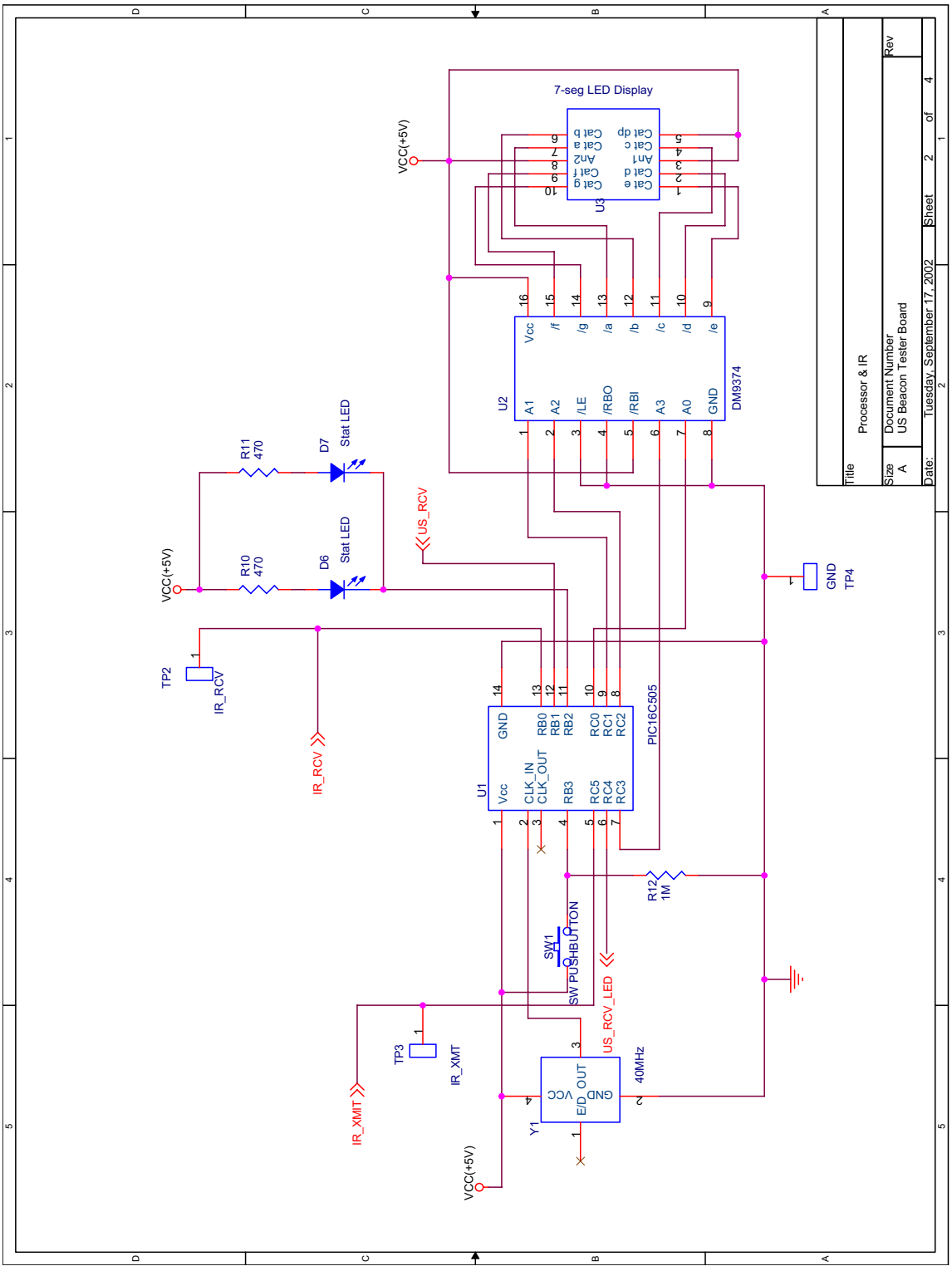

**Figure F.15** Beacon tester functional block diagram

The beacon tester has a manual push-button used to command an IR transmission, equivalent of a satellite starting a global metrology cycle. If the beacon tester receives infrared or

ultrasound signals when the push button has not been operated, it indicates an error (extraneous signals) by showing an E in the display. If the button is pressed and the beacon tester receives a valid ultrasound signal it will display the beacon number (1-9). If the beacon receives too many ultrasound signals or no signal at all, it will indicate an error (E). Any time an ultrasound signal is received the tester flashes the blue LEDs. Whenever an infrared signal is received the beacon tester flashes the green status LEDs. An amber LED indicates a low-battery condition.

## Schematics


All the grounds in this diagram must be one single thick trace which connects the 470uF cap to the IRL520N
VCC(+5V)
R1 100 Ohm
C1 0.1uF
C2 47uF
IR LED D2
IR LED D1
R4 1 Ohm
R3 1 Ohm
D3
IRLML2502
R5 1M
IR_XMIT
IR_XMIT
R7 470
R6 470
D5 US LED
D4 US LED
US_RCV_LED
TP1
US_RCV
US_RCV
US_RCV
US Signal
US-1
US Circuit
C4 0.1uF
C3 4.7uF
IR_RCV
R2 47
J1
IR PAD
VCC(+2.5V)
VCC(+5V)
R8 22K
R9 22K
C5 4.7uF
bypass
Title
Board Assembly
Size A
Document Number US Beacon Tester Board
Rev
Date: Tuesday, September 17, 2002
Sheet 1 of 4


7-seg LED Display
U3
Cat dp
Cat c
Ant1
Cat d
Cat e
Cat a
Ant2
Cat f
Cat g
Cat b
VCC(+5V)
U2
DM9374
Vcc
/f
/g
/a
/b
/c
/d
/e
A1
A2
/LE
/RBO
/RBI
A3
A0
GND
R11
470
D7
Stat LED
R10
470
D6
Stat LED
US_RCV
TP4
TP2
IR_RCV
U1
PIC16C505
GND
RB0
RB1
RB2
RC0
RC1
RC2
Vcc
CLK_IN
CLK_OUT
RB3
RC5
RC4
RC3
R12
1M
SW1
SW PUSHBUTTON
US_RCV_LED
TP3
IR_XMT
IR_XMIT
Y1
GND
VCC
E/D
OUT
40MHz
Title
Processor & IR
Size
A
Document Number
US Beacon Tester Board
Rev
Date:
Tuesday, September 17, 2002
Sheet
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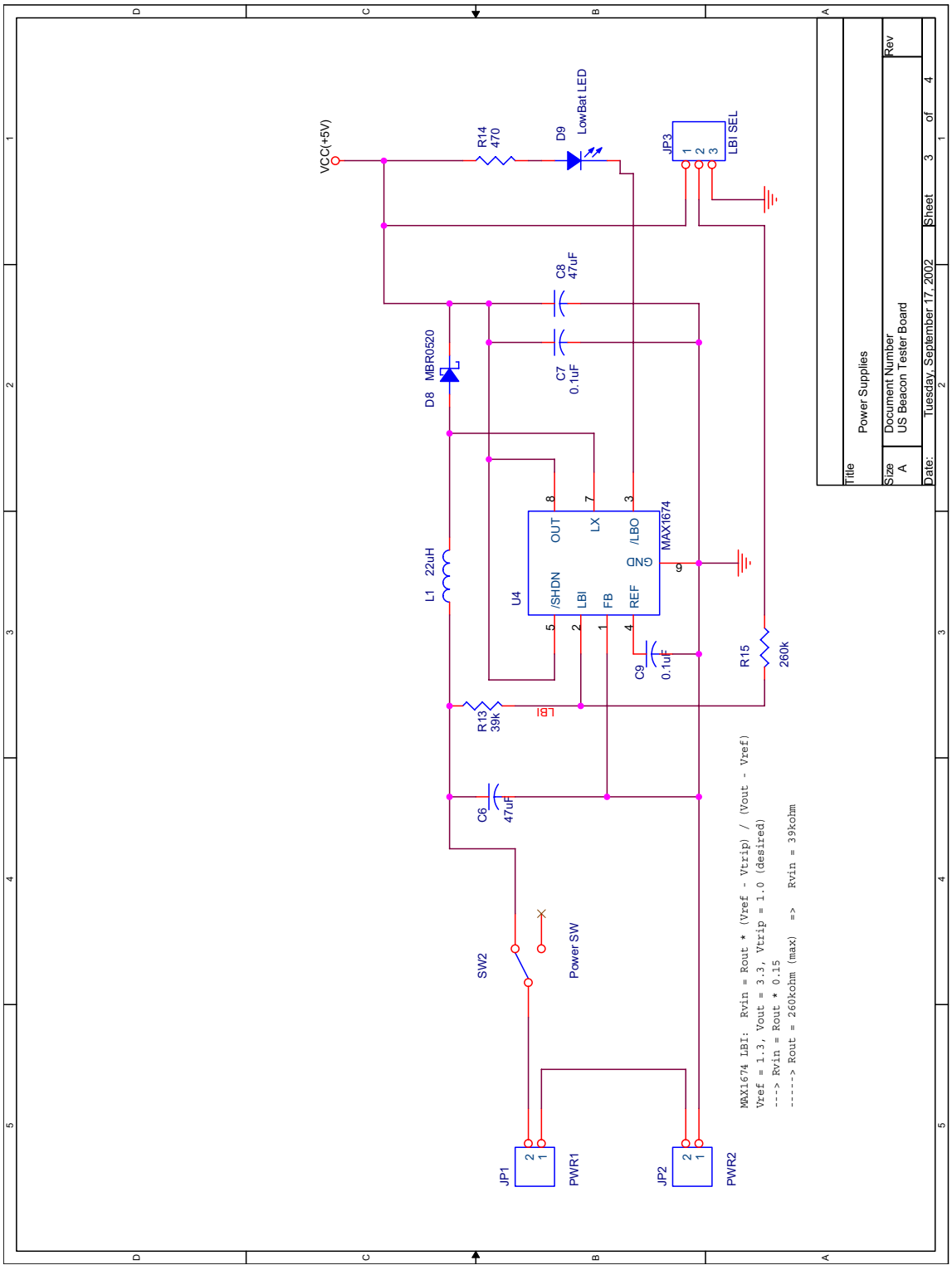
4


VCC(+5V)
R14
470
D9
LowBat LED
JP3
LBI SEL
C8
47uF
C7
0.1uF
D8 MBR0520
L1 22uH
U4
MAX1674
OUT
LX
/LBO
GND
/SHDN
LBI
FB
REF
C9
0.1uF
R15
260k
R13
39k
LBI
C6
47uF
SW2
Power SW
JP1
PWR1
JP2
PWR2
MAX1674 LBI: Rvin = Rout * (Vref - Vtrip) / (Vout - Vref)
Vref = 1.3, Vout = 3.3, Vtrip = 1.0 (desired)
---> Rvin = Rout * 0.15
-----> Rout = 260kohm (max) => Rvin = 39kohm
Title
Power Supplies
Size
A
Document Number
US Beacon Tester Board
Rev
Date:
Tuesday, September 17, 2002
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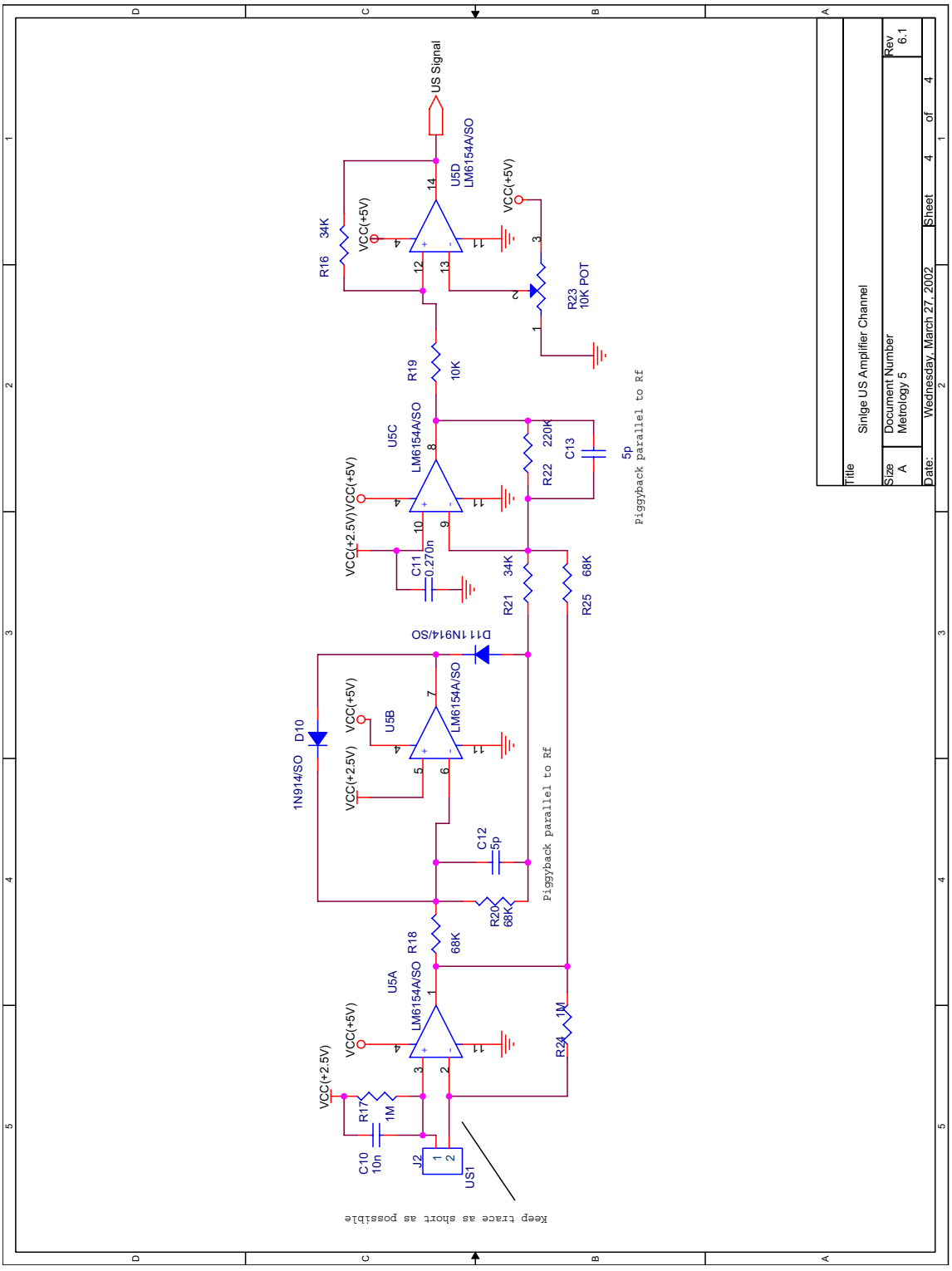
4


US Signal
U5D
LM6154A/SO
VCC(+5V)
R16 34K
R23
10K POT
R19
10K
U5C
LM6154A/SO
R22 220K
C13
5p
Piggyback parallel to Rf
C11
0.270n
VCC(+2.5V)
R21 34K
R25 68K
D11 1N914/SO
D10
1N914/SO
U5B
LM6154A/SO
C12
5p
R20
68K
R18
68K
U5A
LM6154A/SO
R24 1M
R17
1M
C10
10n
J2
US1
Keep trace as short as possible
Title
Sinlge US Amplifier Channel
Size
A
Document Number
Metrology 5
Rev
6.1
Date:
Wednesday, March 27, 2002
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# F.5 Expansion Port Items

## F.5.1 Expansion Port Beacon

The Expansion Port beacon was developed to allow formation flight algorithms where each satellite can transmit an ultrasound signal from two opposite sides: one using the on-board beacon (-X) and another using the expansion port (+X). The expansion port beacon replicates the internal beacon, but uses the serial line in the expansion port instead of it own IR or the use of the IR_rcv_int line which is not available to expansion items. The firmware in the expansion port beacon accounts for the extra delay in serial communications to initiate the command so that the receiving units do not need to account for the delay. The functional block diagram of the expansion port beacon is presented in Figure F.16. Table F.14 describes the inputs and outputs of this expansion item.

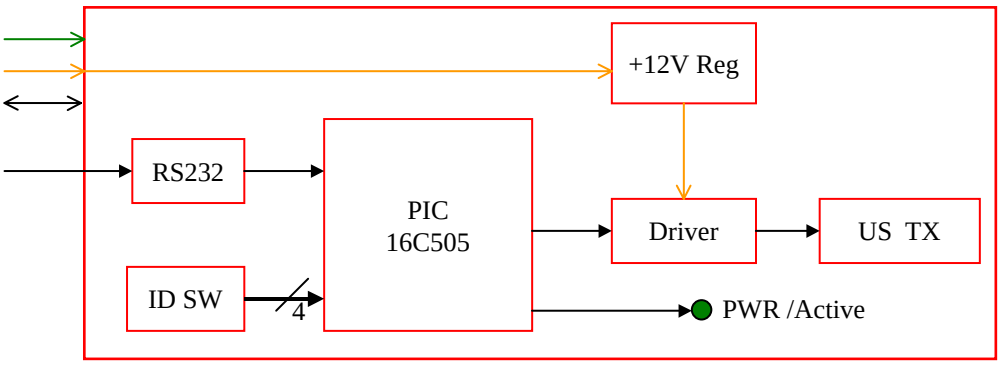
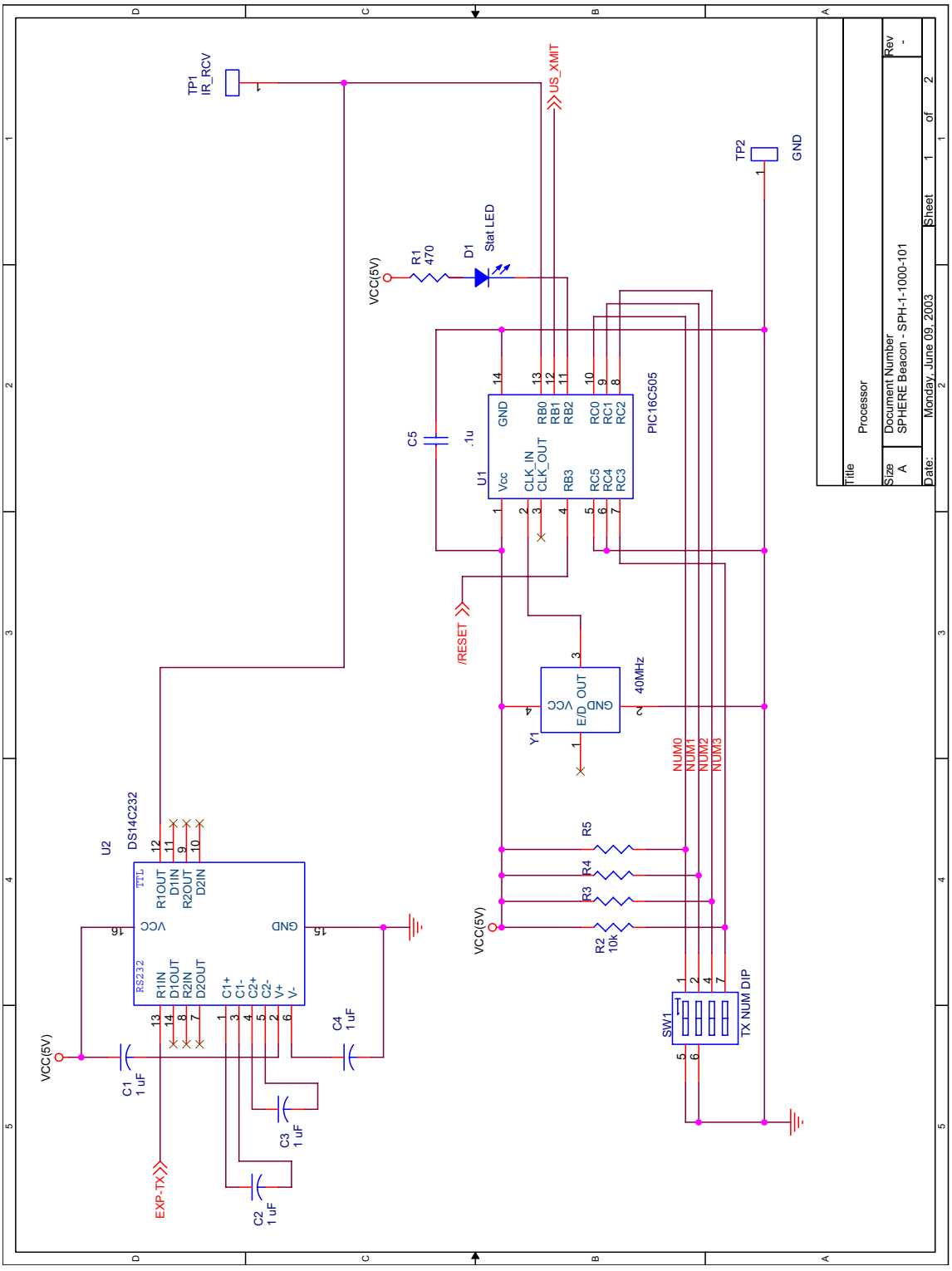



**Figure F.16** Expansion port beacon functional block diagram

**TABLE F.14** Expansion port beacon signals description

| Signal | Type | Description |
|---|---|---|
| Vcc(+5V) | Pwr | +5V power |
| Vcc(+15V) | Pwr | +15V power |
| GND | Pwr | Common Ground |
| TX | In | Transmit data line (RS232) |
| /RESET | In | Reset line |

## Schematics


TP1
IR_RCV
US_XMIT
TP2
GND
VCC(5V)
R1
470
D1
Stat LED
C5
.1u
U1
PIC16C505
GND
Vcc
CLK_IN
CLK_OUT
RB0
RB1
RB2
RB3
RC0
RC1
RC2
RC3
RC4
RC5
/RESET
Y1
40MHz
E/D OUT
NUM0
NUM1
NUM2
NUM3
R5
R4
R3
R2
10k
SW1
TX NUM DIP
U2
DS14C232
TTL
RS232
R1OUT
D1IN
R2OUT
D2IN
R1IN
D1OUT
R2IN
D2OUT
C1+
C1-
C2+
C2-
V+
V-
VCC
GND
C1
1 uF
C2
1 uF
C3
1 uF
C4
1 uF
EXP-TX
Title
Processor
Size
A
Document Number
SPHERE Beacon - SPH-1-1000-101
Rev
-
Date:
Monday, June 09, 2003
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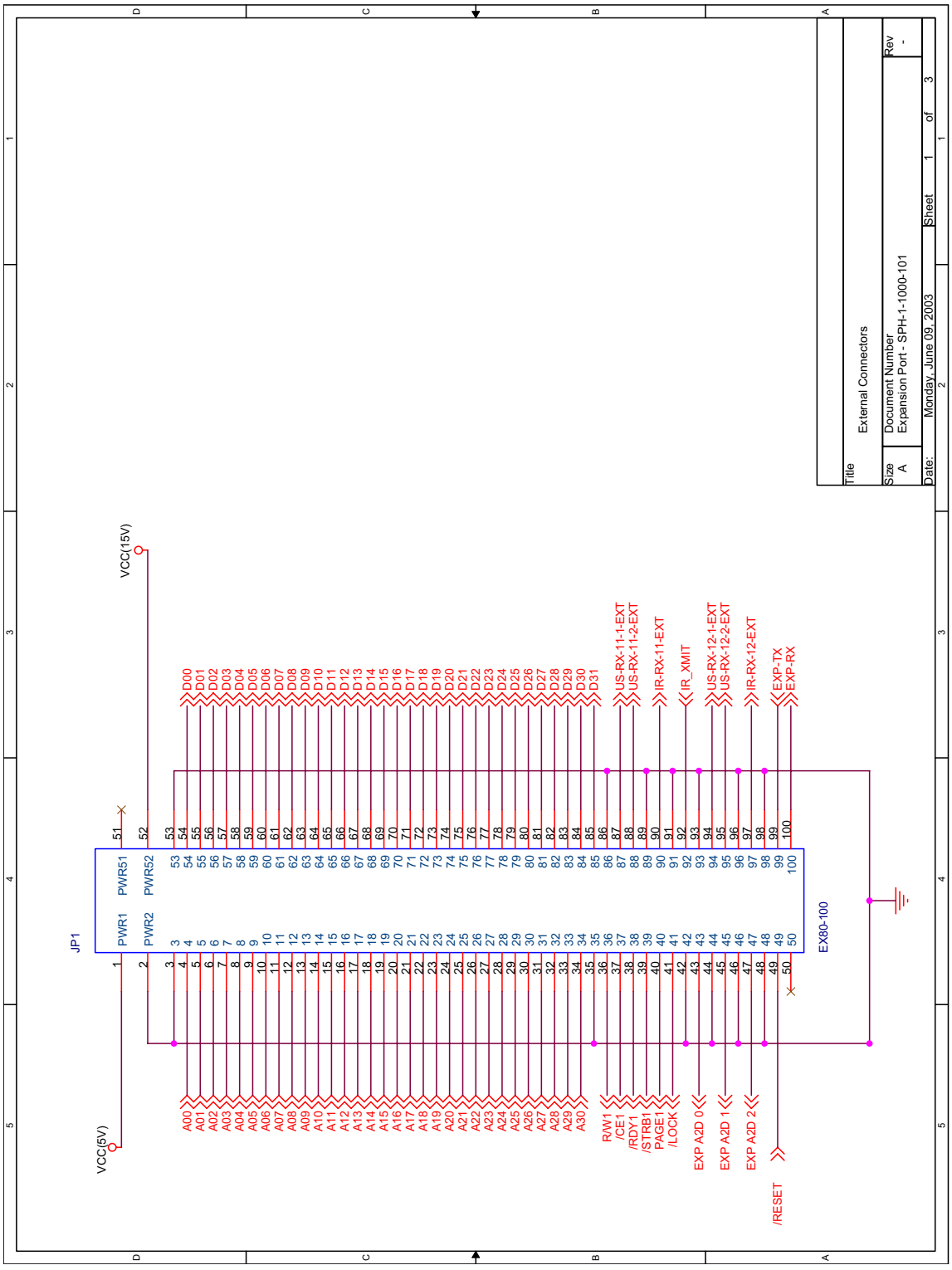
JP1
PWR1
PWR2
PWR51
PWR52
EX80-100
VCC(5V)
VCC(15V)
A00
A01
A02
A03
A04
A05
A06
A07
A08
A09
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
A30
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
R/W1
/CE1
/RDY1
/STRB1
PAGE1
/LOCK
EXP A2D 0
EXP A2D 1
EXP A2D 2
/RESET
US-RX-11-1-EXT
US-RX-11-2-EXT
IR-RX-11-EXT
IR_XMIT
US-RX-12-1-EXT
US-RX-12-2-EXT
IR-RX-12-EXT
EXP-TX
EXP-RX
Title
External Connectors
Size
A
Document Number
Expansion Port - SPH-1-1000-101
Rev
-
Date:
Monday, June 09, 2003
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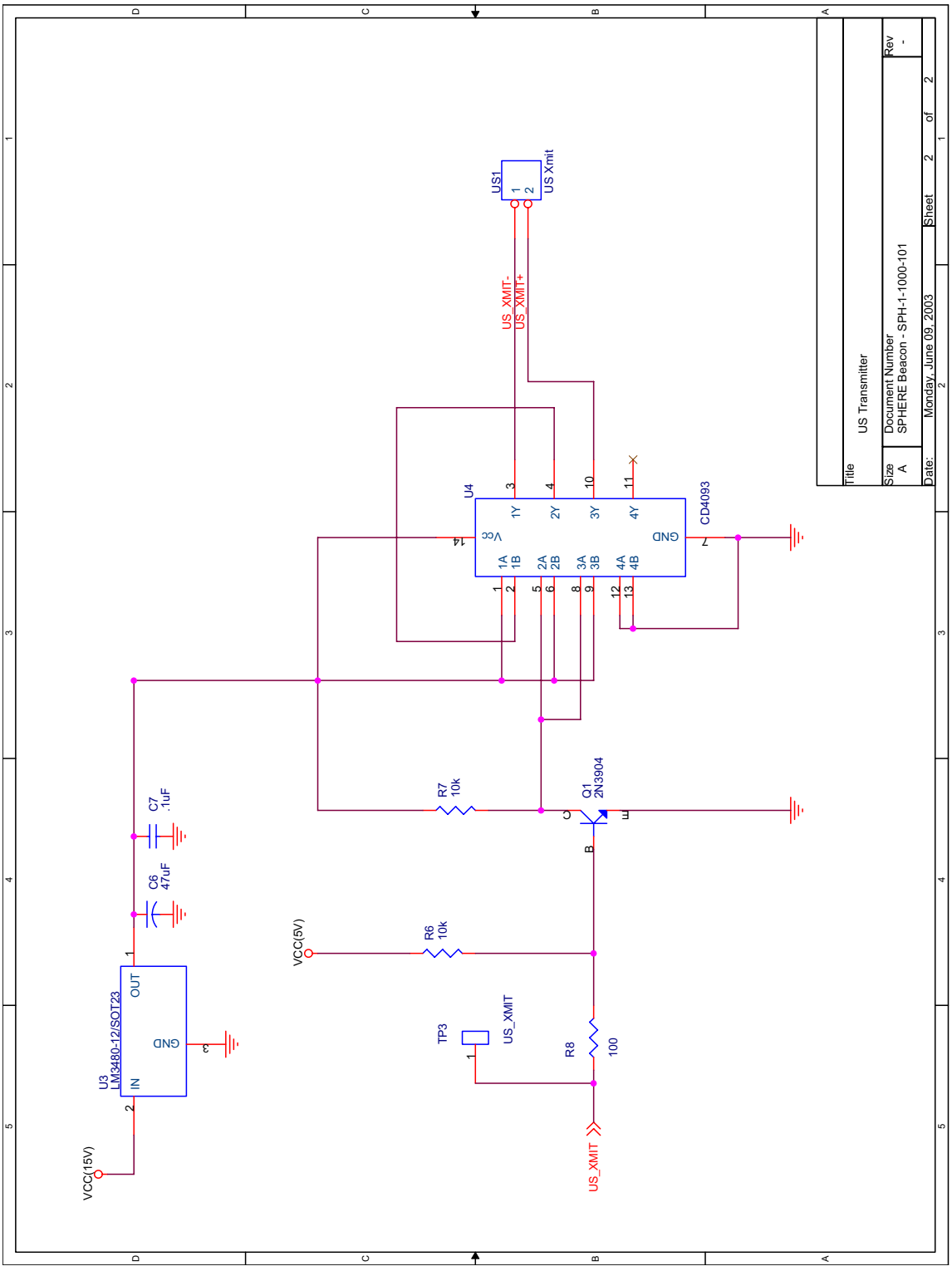
3


US1
US Xmit
US_XMIT-
US_XMIT+
U4
CD4093
1Y
2Y
3Y
4Y
Vcc
GND
1A
1B
2A
2B
3A
3B
4A
4B
R7
10k
Q1
2N3904
C7
.1uF
C6
47uF
U3
LM3480-12/SOT23
OUT
GND
IN
VCC(15V)
VCC(5V)
R6
10k
TP3
US_XMIT
R8
100
US_XMIT
Title
US Transmitter
Size
A
Document Number
SPHERE Beacon - SPH-1-1000-101
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Monday, June 09, 2003
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## F.5.2 Expansion Port Tether

The Expansion Port Tether mechanism is a prototype system to test control algorithms for tethered formation flight spacecraft. The mechanism uses the expansion port serial line to interface with a COTS pulse-width-modulation driver board, which drives a motor to extend or retract a monofilament tether which connects two satellites. This prototype does not have any sensors, allowing the design to be very simple.

Figure F.17 shows the functional block diagram of the expansion port tether board. The board uses a SMC02B micro serial motor controller by Pololu Corporation ([Pololu, URL]). A serial line commands the micro controller the speed and direction of the motor. An adjustable (manual) voltage regulator in the expansion board allows testing of several motors at voltage ranges between 6.5V to 9V. Table F.15 describes the expansion port signals used by the expansion tether board.

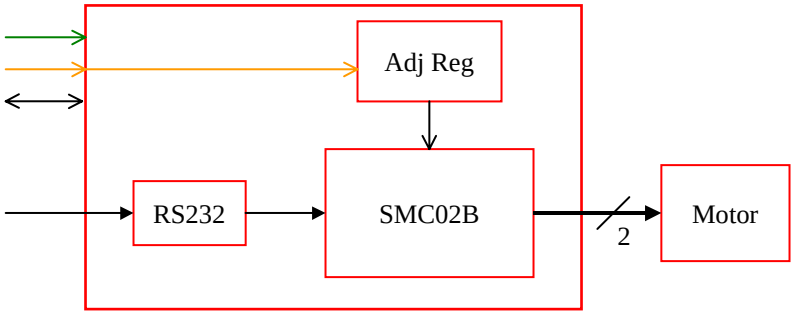
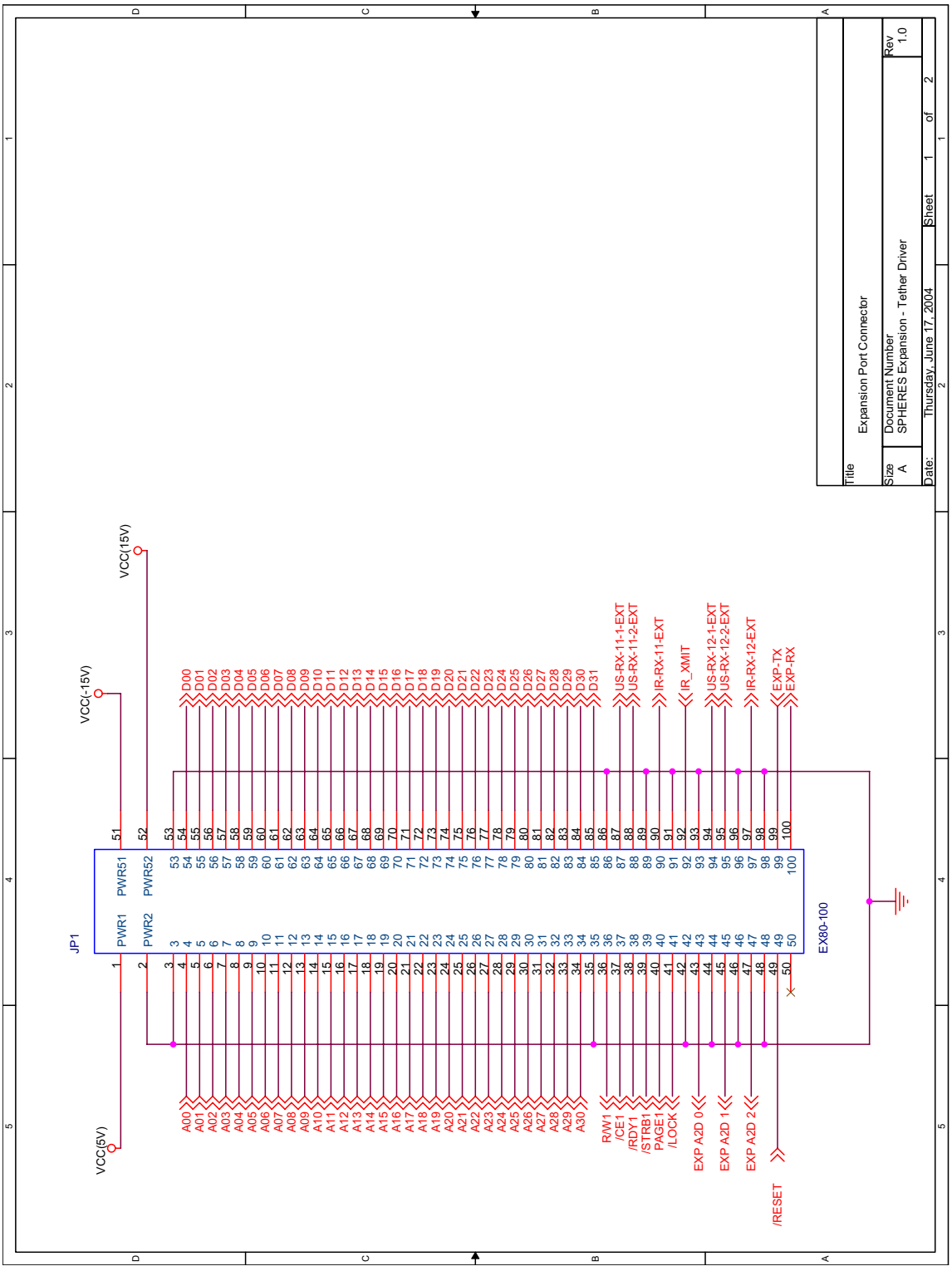



**Figure F.17** Expansion port tether functional block diagram

**TABLE F.15** Expansion port tether signals description

| Signal | Type | Description |
|---|---|---|
| Vcc(+5V) | Pwr | +5V power |
| Vcc(+15V) | Pwr | +15V power - regulated to +7V for motor |
| GND | Pwr | Common Ground |
| TX | In | Transmit data line (RS232) |
| /RESET | In | Reset line |

## Schematics


Expansion Port Connector
Document Number
SPHERES Expansion - Tether Driver
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A
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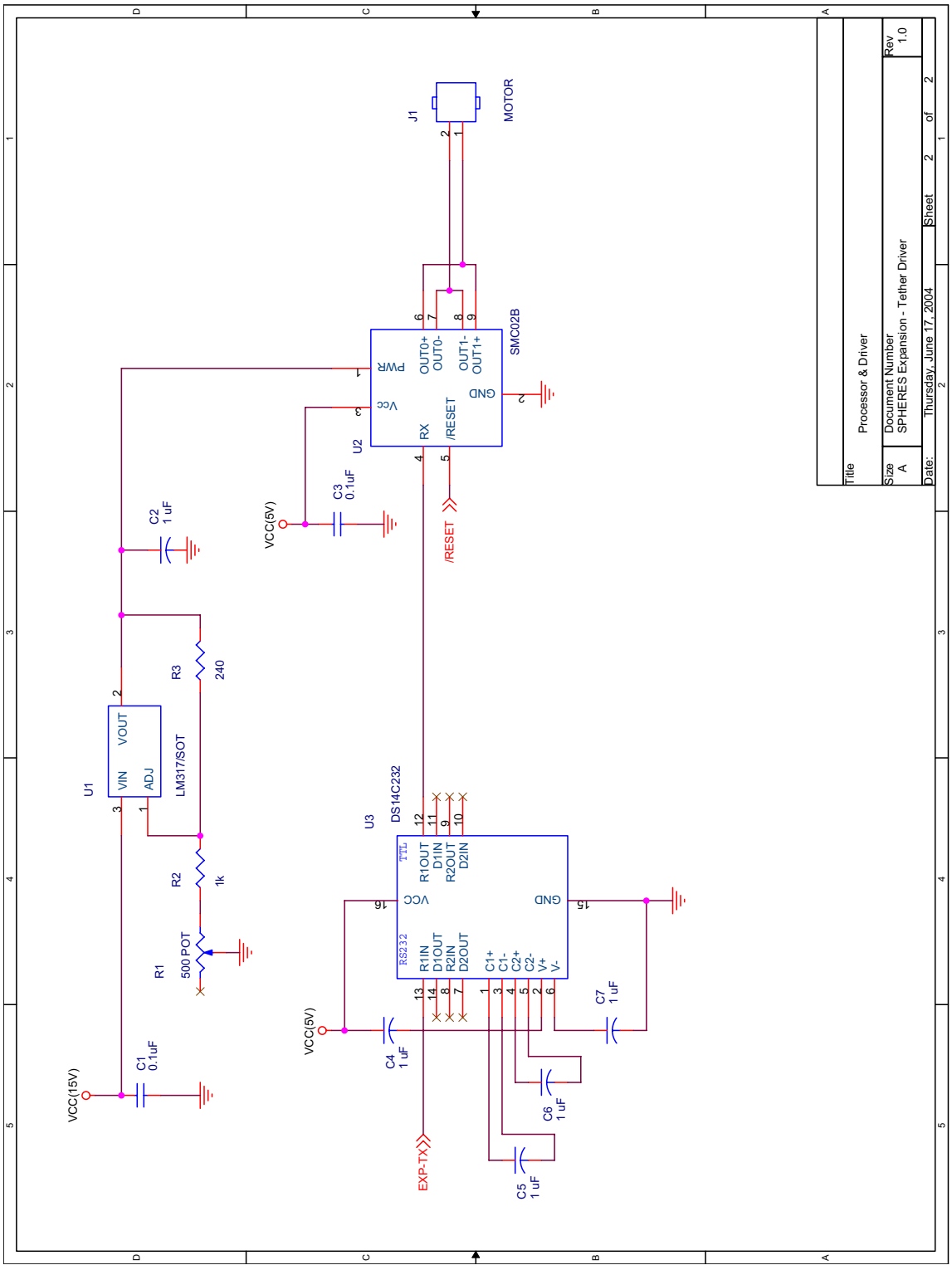
Sheet
1
of
2
JP1
EX80-100
VCC(-15V)
VCC(15V)
VCC(5V)
PWR1
PWR2
PWR51
PWR52
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
A00
A01
A02
A03
A04
A05
A06
A07
A08
A09
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
A24
A25
A26
A27
A28
A29
A30
US-RX-11-1-EXT
US-RX-11-2-EXT
IR-RX-11-EXT
IR_XMIT
US-RX-12-1-EXT
US-RX-12-2-EXT
IR-RX-12-EXT
EXP-TX
EXP-RX
R/W1
/CE1
/RDY1
/STRB1
PAGE1
/LOCK
EXP A2D 0
EXP A2D 1
EXP A2D 2
/RESET


J1
MOTOR
U2
SMC02B
PWR
OUT0+
OUT0-
OUT1-
OUT1+
GND
Vcc
/RESET
RX
C3
0.1uF
VCC(5V)
/RESET
C2
1 uF
U1
LM317/SOT
VIN
VOUT
ADJ
R3
240
R2
1k
R1
500 POT
C1
0.1uF
VCC(15V)
U3
DS14C232
TTL
RS232
R1OUT
D1IN
R2OUT
D2IN
R1IN
D1OUT
R2IN
D2OUT
VCC
GND
C1+
C1-
C2+
C2-
V+
V-
C4
1 uF
C5
1 uF
C6
1 uF
C7
1 uF
EXP-TX
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Processor & Driver
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